

**Anritsu** Advancing beyond

# Signal Quality Analyzer-R

PCIe/USB/Thunderbolt/Display Port Test Solutions\*

## MP1900A

**SQA-R**



\*: Refer to the 32G/64G NRZ/PAM4 Signal Integrity Test Solution Catalog (MP1900A\_64G-E-A-1) for the information on MP1900A PAM4 test solution.



# Support 400 GbE/800 GbE and PCIe Gen5/6

Due to the explosive growth of data traffic resulting from the popularity of smartphones and mobile terminals, network interfaces are transitioning to faster 400 GbE/800 GbE standards, and PCI bus interface speeds now exceed 64G. In addition, the equipment and chipsets using these interfaces support multi-channels and multi-protocols. The MP1900A is a high-performance BERT with excellent expandability for supporting Physical layer evaluations of these high-speed interfaces. The all-in-one design is ideal for early stage R&D evaluations of all interfaces covering next-generation Ethernet networks to bus interconnects.

## MP1900A Signal Quality Analyzer-R



Certified for  
PCIe Gen 3/4/5/6  
USB3.2/4 v1  
Thunderbolt3/4  
DP1.4/2.0/2.1

PCIe/USB3.2  
Sequence Editor  
for  
Troubleshooting

USB4 v2  
USB3.2 ×2  
Compliance Test  
Ready

### Excellent Expandability

All-in-one support for both high-speed Ethernet and PCI Express interface tests

Supports transmissions up to 512 Gbit/s

- 32G bandwidth : 8ch NRZ, 4ch PAM4
- 64G bandwidth : 4ch NRZ, 4ch PAM4

8 slots for adding extra modules

Backwards compatibility with MP1800A series modules

### Link Training

Receiver tests are supported by the built-in Protocol Awareness PCIe Link Training, USB Link Training and LTSSM analysis functions.

Supports PCI Express Gen 1/2/3/4/5/6  
Supports both USB 3.2 Gen1/2 ×1 and ×2

Supports Link Training troubleshooting using Sequence Editor

### Signal Integrity Evaluation

10Tap Emphasis built-in

Variable ISI Function

Multi-band CTLE

CDR Function (supports SSC)

Jitter Addition (SJ/RJ/BUJ/SSC) function

User-defined SSC profile function

Voltage Noise Addition (CM/DM/Gaussian) function

### High Waveform Quality and High Sensitivity

Low Intrinsic (Residual) Jitter output (115 fs rms)

High-sensitivity Data input (15 mV)

Operation bit rates from 2.4 Gbit/s to 32.1 Gbit/s



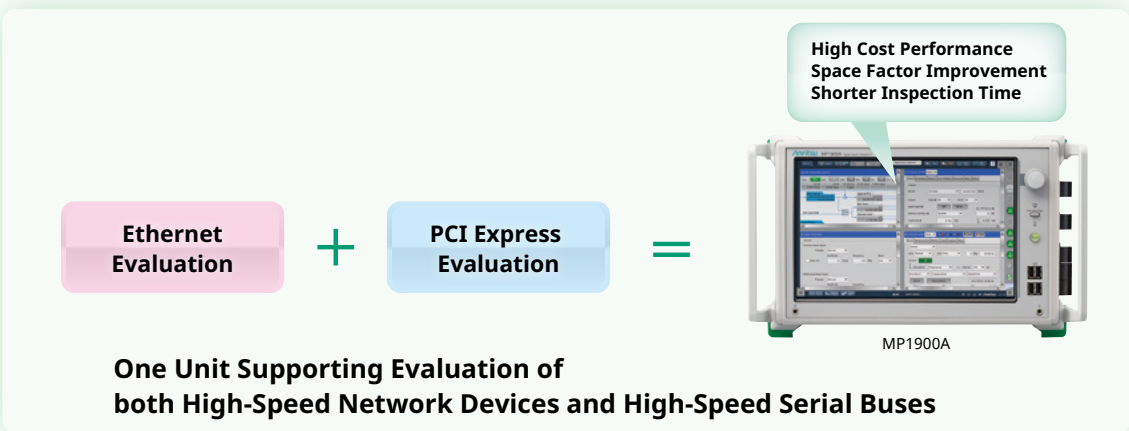
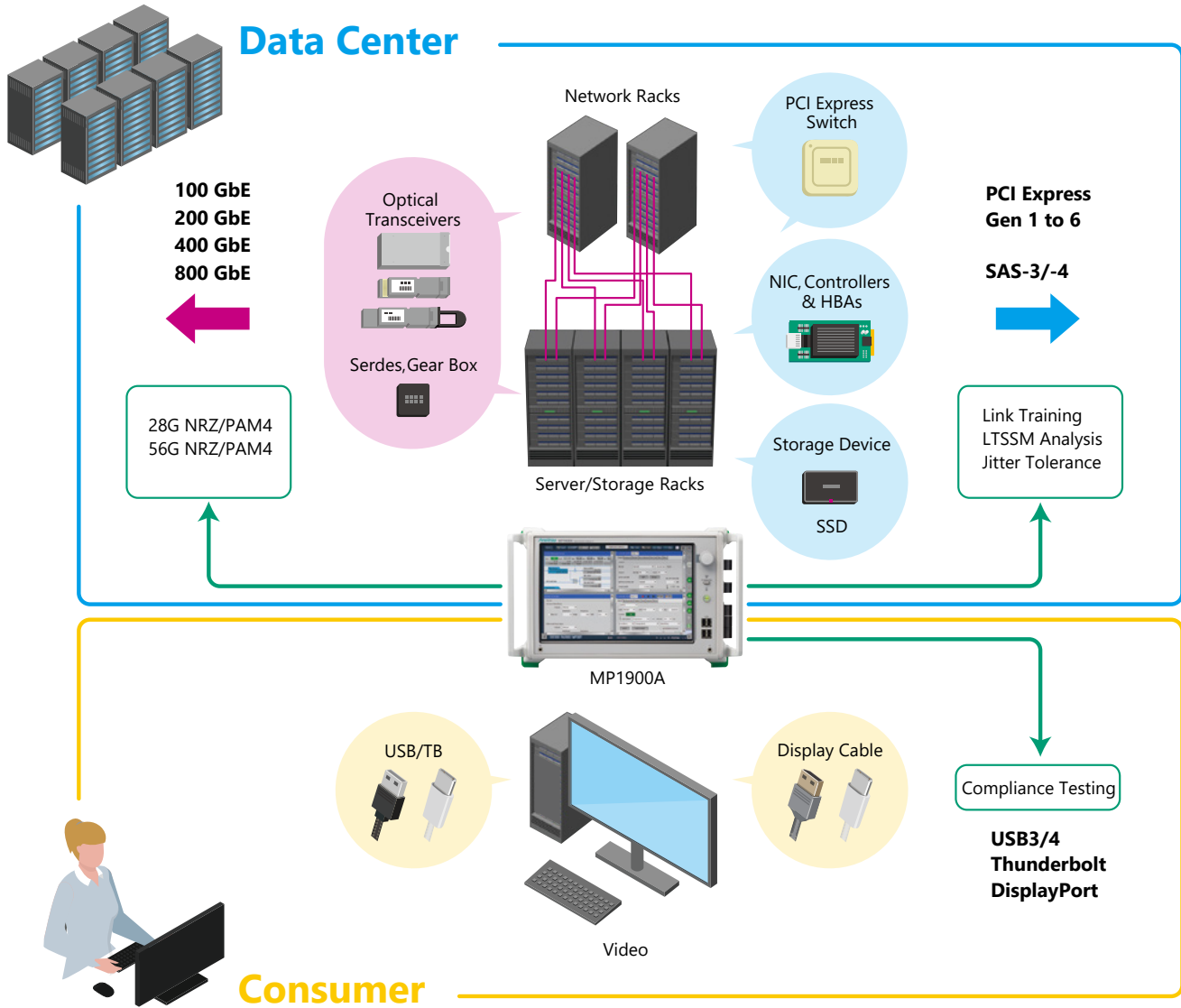
## Wide Application Support

100 GbE/200 GbE/400 GbE/800 GbE, CEI-25G/28G/56G/112G, InfiniBand EDR/HDR, Fibre Channel PCI Express Gen 1/2/3/4/5/6, Thunderbolt 1/2/3/4, USB3.2/4 v1/4 v2, SAS-3/-4, DP1.4/2.0/2.1 Optical module, SERDES, AOC, High-speed Interconnect 3

# Excellent Expandability

## All-in-One Support for Evaluating Next-Generation NRZ/PAM4 Network Interfaces and High-Speed Serial Buses

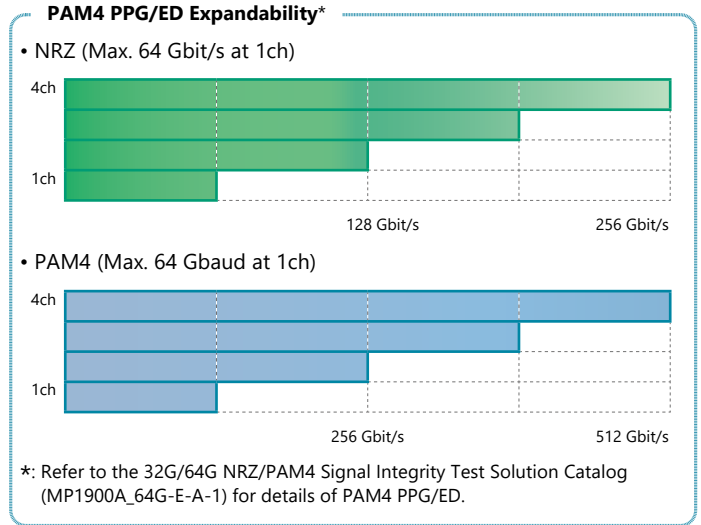
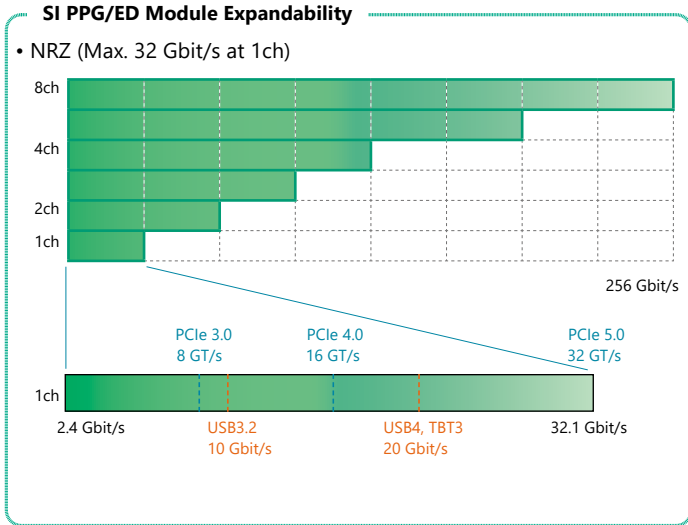
The Signal Quality Analyzer–R MP1900A is a modular Bit Error Rate Tester (BERT) supporting equipment external interfaces, such as next-generation Ethernet, by installing a pulse pattern generator (PPG) for outputting high-quality multi-channel NRZ/PAM4 signals over a wide bandwidth, a high-sensitivity input error detector (ED), Jitter modulation sources for Jitter Tolerance tests, etc. Additionally, optional noise generation and 10Tap Emphasis functions can be installed for Voltage Noise Tolerance tests, etc., and installing the High-Speed Serial Data Test Software software enables efficient design evaluation for increasingly faster PCIe, USB, Thunderbolt, SAS and DP receivers.



# Excellent Expandability

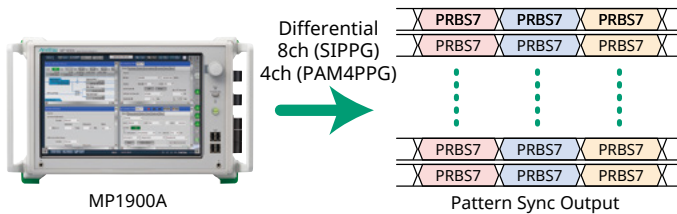
## Easy Flexibility for Multi-Channel Measurements at Various Transmission Rates and Formats

400 GbE is the standard for the next generation of large-capacity transmissions but it is still unknown how much further data traffic will grow. To cope with this data traffic growth, in addition to speeding-up NRZ signals and introducing multi-channel signalling, introduction of PAM4-format signals is also progressing. To facilitate this change to multi-channels and the new PAM4 signals, the MP1900A series is an 8-slot modular instrument that can be easily customized by selecting and adding required function modules. This flexible expandability supporting the latest communications methods ensures both efficient R&D investment and the fastest time to market.



In addition to installing PPG, ED, and noise-generation modules in the 8-slot main unit, existing modules for the previous MP1800A series can also be installed. A combined total of up to four PPG and ED modules can be mounted in one MP1900A. The 21G/32G bit/s SI PPG/ED modules support selection of both one and two channels, enabling up to 8-channel measurement for both the PPG and ED. The PAM4 PPG and ED modules are configured with one channel per module, allowing up to four PPG or ED channels to be implemented simultaneously in one main unit. Moreover, the pattern for each channel can be synchronized, providing an ideal solution for evaluating DAC, MUX and DEMUX devices as well as for crosstalk and skew tolerance tests.

\*: Refer to the MP1900A Selection Guide (MP1900A-E-Z-1) for details of the supported multi-channel configurations and module combinations. Consult our business sales representative for use of other module configurations not described in the MP1900A Selection Guide.



# Multi Interface

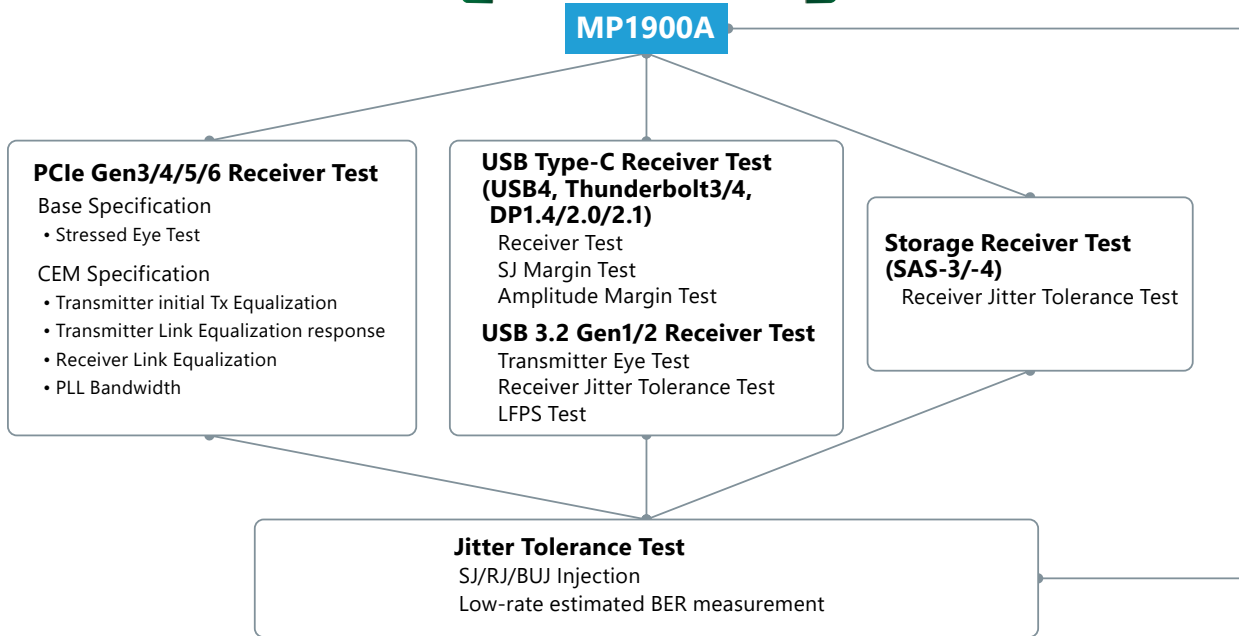
## Next-Generation High-Speed Digital Interface Receiver Test

The growth of IoT and Cloud computing applications is driving the need for digital equipment with high-speed serial interfaces handling large data volumes. To meet this need, the PCI Express (PCIe) and USB interfaces used by this digital equipment are transitioning to both next-generation PCIe Gen6 supporting speeds up to 64 GT/s as well as to Type-C USB3.2 Gen2 supporting 10 Gbit/s and USB4 supporting 20 Gbit/s, which is also compatible with Thunderbolt.

The MP1900A is a wideband BERT with a built-in Gbit/s-class PPG, ED, and Jitter/Noise addition functions as well as application software supporting measurement of next-generation, high-speed digital-interface standards (CEI-28G/56G/112G, InfiniBand, 100G/400G/800G Ethernet, Fibre Channel, Thunderbolt, PCIe, USB, SAS, DP) from development through to manufacturing.



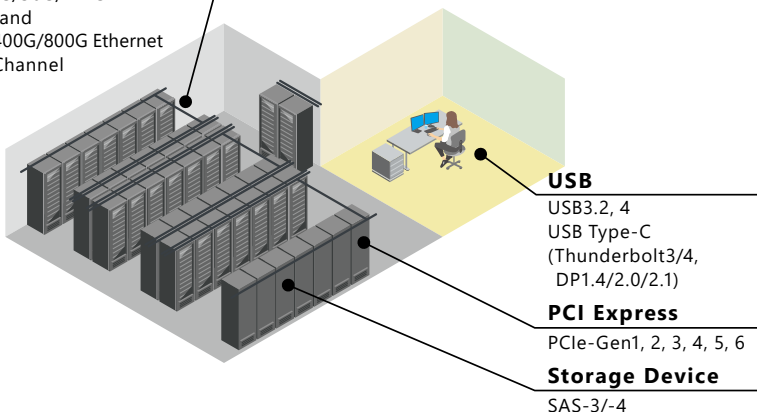
**All-in-One  
Test Support**



## Target Applications

### General Interfaces

CEI-28G/56G/112G  
InfiniBand  
100G/400G/800G Ethernet  
Fibre Channel



### Various Applications

Internal and external interfaces, such as Ethernet, PCIe, and SAS, are supported along with USB3.2, 3.4, and Thunderbolt via USB Type-C connectors and cables, and Display Port.

MP1900A supports PCIe 3.0, 4.0, 5.0 and 6.0 as well as SAS using the same configuration.

# Full Automation

## Full Automation Software

Automation software for automating receiver tests of high-speed serial bus interfaces controls the MP1900A (PPG/ED, noise signal source, variable ISI channel) and real-time oscilloscope to automate calibration of signals required for complex operations, Jitter Tolerance tests, and creation of reports. The high-reproducibility, easy measurements greatly reduce the work load of test engineers.

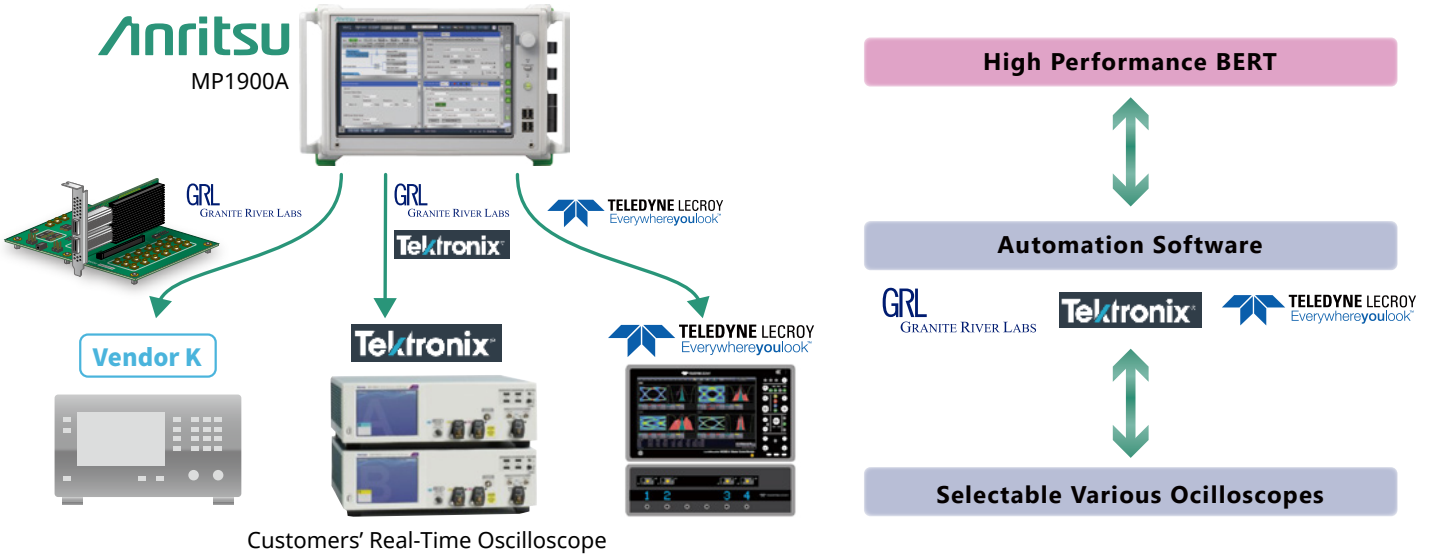
### Features

- Controls each measuring instrument to simplify calibration, measurement conditions settings, and test execution
- Calibrates test signal and executes receiver test with high reproducibility
- Automates standards-compliant Jitter and amplitude Pass/Fail evaluations
- Selectable Various Oscilloscope

### Selectable Various Oscilloscope

Real-time oscilloscopes from the main makers can be used in combination with the MP1900A to calibrate test signals, helping cut capital investment costs by making efficient use of owned assets.

Refer to the Selection Guide (MP1900A-E-Z-1) for the combination of supported real-time oscilloscopes and automation software.



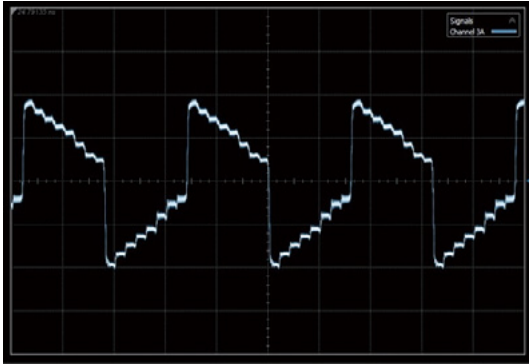
# SI PPG/ED Signal Integrity Evaluation

## Strengthened Signal Integrity Evaluations in Addition to New SI PPG, SI ED and Noise Generator Modules

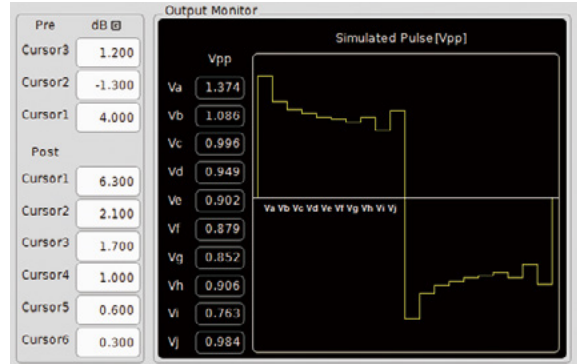
Emphasis and equalizer functions are built-in to correct transmission path losses and assure signal integrity as signals become faster and as high-speed devices use lower signal levels to help reduce power consumption.

### 10Tap Emphasis

The 10Tap Emphasis option installed in the transmission-side 21G/32 Gbit/s SI PPG MU195020A can accurately replay simulated waveforms for various devices and channels (corrected for loss after passage through channel) to help improve design efficiency.



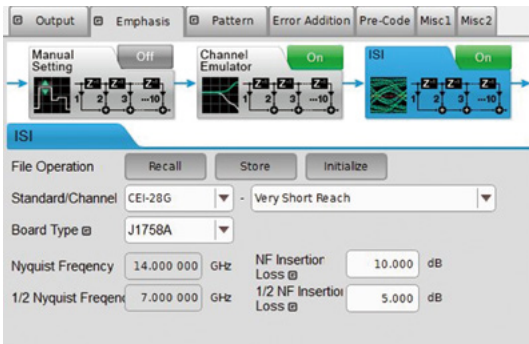
Waveform adjustment using 10Tap Emphasis Function



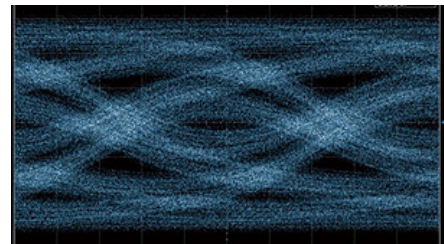
Emphasis Setting Screen Example

Additionally, the Variable ISI (option) can generate a signal with simulated Loss between the Tx and Rx channels of high-speed devices by setting the channel Loss for the frequencies defined in CEI-28 G/25G and the S-parameter information, and can also easily output a Loss-corrected waveforms. As a result, channel-Loss dependent high-speed device performance tests can be run easily with good reproducibility without needing to prototype multiple channel boards, helping cut development time.

\* For Variable ISI (option), use either in combination with ISI Board J1758A (select J1758A) or in combination with external channel board (select Not Specified).



ISI Setting Screen Example

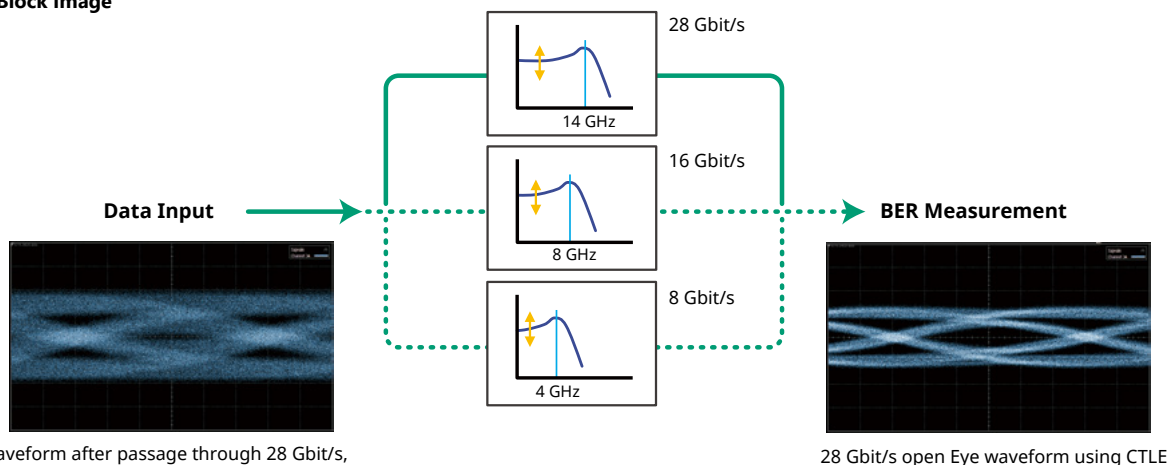


ISI, CEI-28G, 14 dB Loss waveform (typical)

### Multi-band CTLE

Installing the CTLE option supporting multi-band input signals of 28, 16, and 8 Gbit/s at the receive-side of the 21G/32G bit/s SI ED MU195040A permits BER measurements even when the Eye is closed by transmission path losses. Since this CTLE function is a hardware equalizer rather than the software emulator, it supports evaluation of TRX BER performance under near-to-live conditions, such as BER evaluation of test signals, and comparison of DUT BER measurement results.

#### 3-band CTLE Block Image



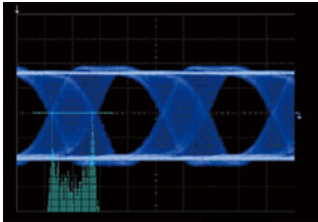
Waveform after passage through 28 Gbit/s, -10 dB @ 14 GHz channel

28 Gbit/s open Eye waveform using CTLE

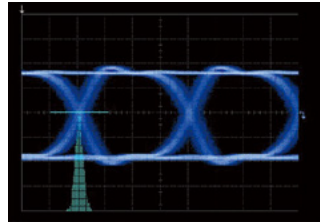
# SI PPG/ED Signal Integrity Evaluation

## Jitter/Noise Addition

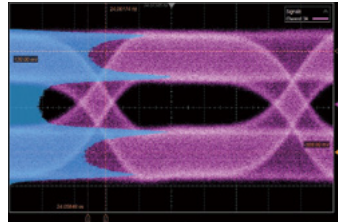
To perform DUT receiver stressed input tolerance tests, the BER is measured under the worst conditions using a stressed signal with added jitter and voltage noise. Using the MP1900A series with the Jitter Modulation Source MU181500B, Jitter Tolerance Test MX183000A-PL001 software, and Noise Generator MU195050A for adding CM/DM/White Noise supports receiver tolerance tests in conformance with the various interface standards. The MP1900A series offers strong support for receiver stressed input tolerance tests by generating high-quality signals before jitter and noise addition as well as for adding high-linearity jitter and noise.



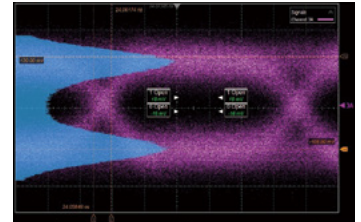
Sinusoidal Jitter (SJ)



Random Jitter (RJ)



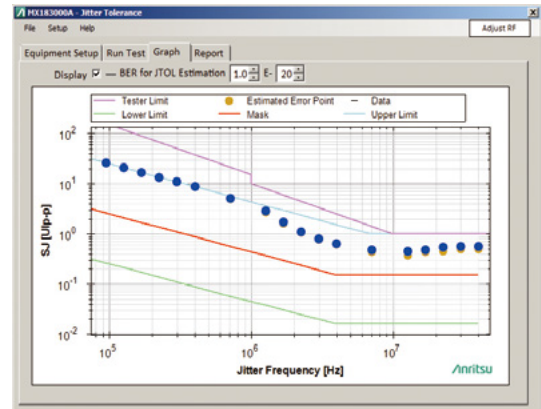
CM/DM Noise



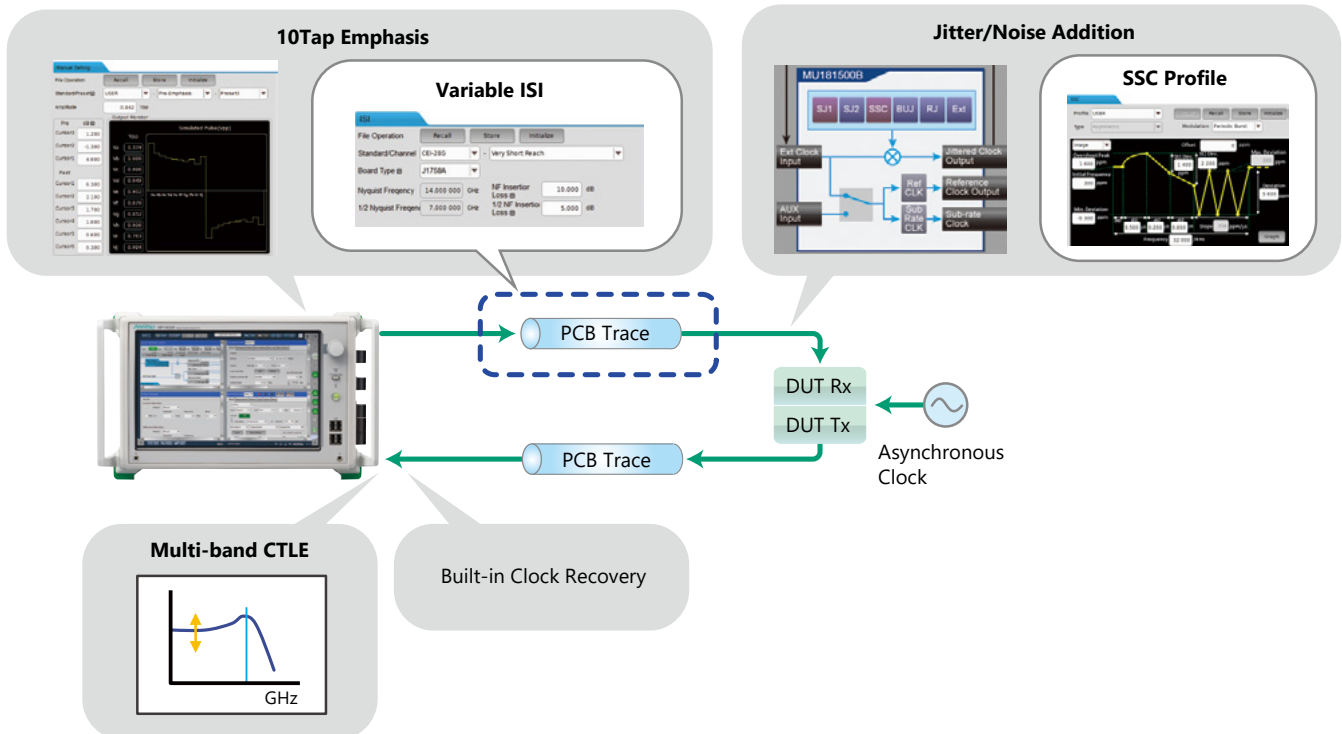
White Noise

## Jitter Tolerance Test Function (MX183000A-PL001)

- High-versatility Jitter Tolerance measurements
- PHY Device Jitter Tolerance tests by impressing SJ/RJ/BUJ
- Standards-compliant Mask measurements
- Fast measurement times using low error rate estimation function, such as 1E-12 and 1E-15
- Tolerance measurements versus device characteristics using four Binary, Upward, Downward, Binary + Linear methods



Low Error Rate Estimation BER Measurements



# SI PPG/ED Link Training (PCIe Gen1 to 5)

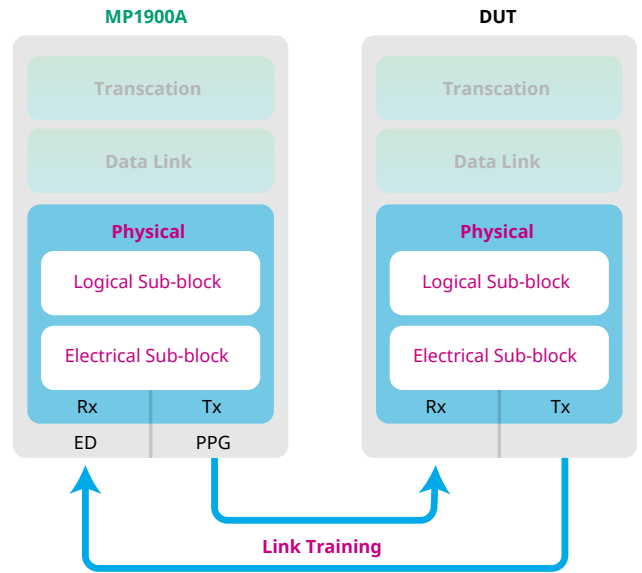
The PCI Express and 10 Gbit/s USB3.2 standards require PHY layer tests such as Jitter Tolerance tests on an established Link to assure interconnectivity between the host and device. Additionally, it is necessary to determine whether the cause is a physical or logical fault at a Link fault.

The MP1900A PCI Express/USB functions have Protocol Awareness with a Link Training function required for evaluating the PHY layer as well as an analysis function for detecting each LTSSM state transition to help troubleshoot faults. When more detailed debugging is required, the training sequence generation timing can be adjusted using the Sequence Editor function (MU195020A-x50/x51).

These all-in-one functions facilitate efficient PHY layer evaluation of PCIe Gen1 to Gen5 and USB3.2 receivers through inspection and fault troubleshooting.

Moreover, combination with the Jitter Tolerance Measurement function (MX183000 A-PL001) supports consistent receiver tests of high-speed serial interfaces.

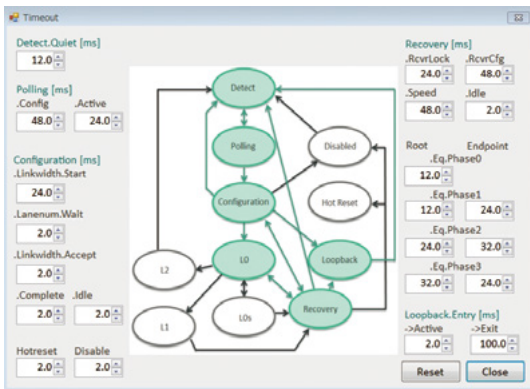
LTSSM: Link Training Status State Machine



Supports physical layer measurements of add-in cards and system boards

- Tx LEQ: Transmitter Link Equalization response Test
- Rx LEQ: Receiver Link Equalization Test
- Receiver Jitter Tolerance Test

## PCI Express Link Training (MX183000A-PL021/PL025/PL026)

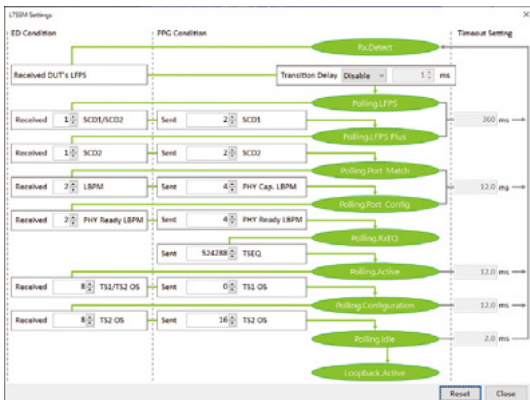


PCIe Link Training State Transition

Time [ms]	ΔTime [ms]	State	Speed[GT/s]	Detect Preset	Error Count	Un Preset	Preset	Pre-out	Counter	Post-counter	Detail
0	0	INITIAL	16.0	---	---	---	---	---	---	---	00:00:00:00:00:00:00:00
13780	13780	DETECT_ACTIVE	16.0	---	---	---	---	---	---	---	00:01:00:06:70:49:07:00:00:00
12817280	12800000	DETECT_ACTIVE	16.0	---	---	---	---	---	---	---	00:01:00:06:44:18:07:00:00:00
12817296	16	POLLING_ACTIVE_T03	16.0	---	---	---	---	---	---	---	00:11:00:05:44:18:07:00:00:00
16917296	24000000	INITIAL	16.0	---	---	---	---	---	---	---	00:00:00:03:2A:0B:07:00:00:00
16917312	16	DETECT_ACTIVE	16.0	---	---	---	---	---	---	---	00:01:00:03:2A:0B:07:00:00:00
40917312	12000000	DETECT_ACTIVE	16.0	---	---	---	---	---	---	---	00:01:00:03:2A:0B:07:00:00:00
40917320	16	POLLING_ACTIVE_T03	16.0	---	---	---	---	---	---	---	00:11:00:03:08:3F:07:00:00:00
72917320	24000000	INITIAL	16.0	---	---	---	---	---	---	---	00:00:00:07:05:01:07:00:00:00
72917344	16	DETECT_ACTIVE	16.0	---	---	---	---	---	---	---	00:01:00:07:05:01:07:00:00:00
84917344	12000000	DETECT_ACTIVE	16.0	---	---	---	---	---	---	---	00:01:00:06:06:16:07:00:00:00
84917360	16	POLLING_ACTIVE_T03	16.0	---	---	---	---	---	---	---	00:11:00:06:06:16:07:00:00:00
108017360	24000000	INITIAL	16.0	---	---	---	---	---	---	---	00:00:00:04:7F:23:07:00:00:00
108017376	16	DETECT_ACTIVE	16.0	---	---	---	---	---	---	---	00:01:00:04:7F:23:07:00:00:00
120017376	12000000	DETECT_ACTIVE	16.0	---	---	---	---	---	---	---	00:01:00:03:62:05:07:00:00:00
120017392	16	POLLING_ACTIVE_T03	16.0	---	---	---	---	---	---	---	00:11:00:03:62:05:07:00:00:00
144017392	24000000	INITIAL	16.0	---	---	---	---	---	---	---	00:00:00:01:24:47:07:00:00:00
144017408	16	DETECT_ACTIVE	16.0	---	---	---	---	---	---	---	00:01:00:01:24:47:07:00:00:00
154017408	12000000	DETECT_ACTIVE	16.0	---	---	---	---	---	---	---	00:01:00:00:0C:A9:07:00:00:00
154017424	16	POLLING_ACTIVE_T03	16.0	---	---	---	---	---	---	---	00:11:00:00:0C:A9:07:00:00:00
180017424	24000000	INITIAL	16.0	---	---	---	---	---	---	---	00:00:00:05:03:0B:07:00:00:00
180017440	16	DETECT_ACTIVE	16.0	---	---	---	---	---	---	---	00:01:00:05:03:0B:07:00:00:00
19017440	12000000	DETECT_ACTIVE	16.0	---	---	---	---	---	---	---	00:01:00:04:06:03:0B:07:00:00:00

LTSSM Log of each LTSSM State Transition

## USB Link Training (MX183000A-PL022/PL023)



USB Link Training State Transition

Time [ms]	ΔTime [ms]	State	Speed[GT/s]	Detail
0	6,945,704	INITIAL	10.0	00:00:00:00:00:00:00:00:00:00
6,945,704	24	DETECT_ACTIVE	10.0	00:02:00:00:00:00:00:00:00:00
6,945,728	69,440	POLLING_LFPS_SCD1	10.0	00:12:00:00:00:00:00:00:00:00
7,015,168	121,864	POLLING_LFPS_PLUS	10.0	00:14:00:00:00:00:00:00:00:00
7,137,032	71,808	POLLING_LFPS_INDICED	10.0	00:15:00:00:00:00:00:00:00:00
7,209,840	39,048	POLLING_PORT_MATCH	10.0	00:16:00:00:00:00:00:00:00:00
7,297,888	110,080	POLLING_PORT_CONFIG_READY	10.0	00:17:00:00:00:00:00:00:00:00
7,407,968	-26,392	POLLING_PORT_ENDLBRM	10.0	00:18:00:00:00:00:00:00:00:00
7,434,360	7,176,248	POLLING_REQ	10.0	00:14:00:00:00:00:00:00:00:00
14,611,608	2,176	POLLING_ACTIVE	10.0	00:18:00:00:00:00:00:00:00:00
14,614,784	2,192	POLLING_CONFIG_MATCH	10.0	00:1C:00:00:00:00:00:00:00:00
14,628,976	24	POLLING_IDLE	10.0	00:1D:00:00:00:00:00:00:00:00
14,637,000	0	LOOPBACK_ACTIVE	10.0	00:64:00:00:00:00:00:00:00:00

LTSSM Log of each LTSSM State Transition

# Sequence Editor (PCIe1 to 6, USB3.2, Multi-channel)

## Sequence Editor (MU195020A-x50/x51, MU196020A-x51/x52, MU196040B-x51)

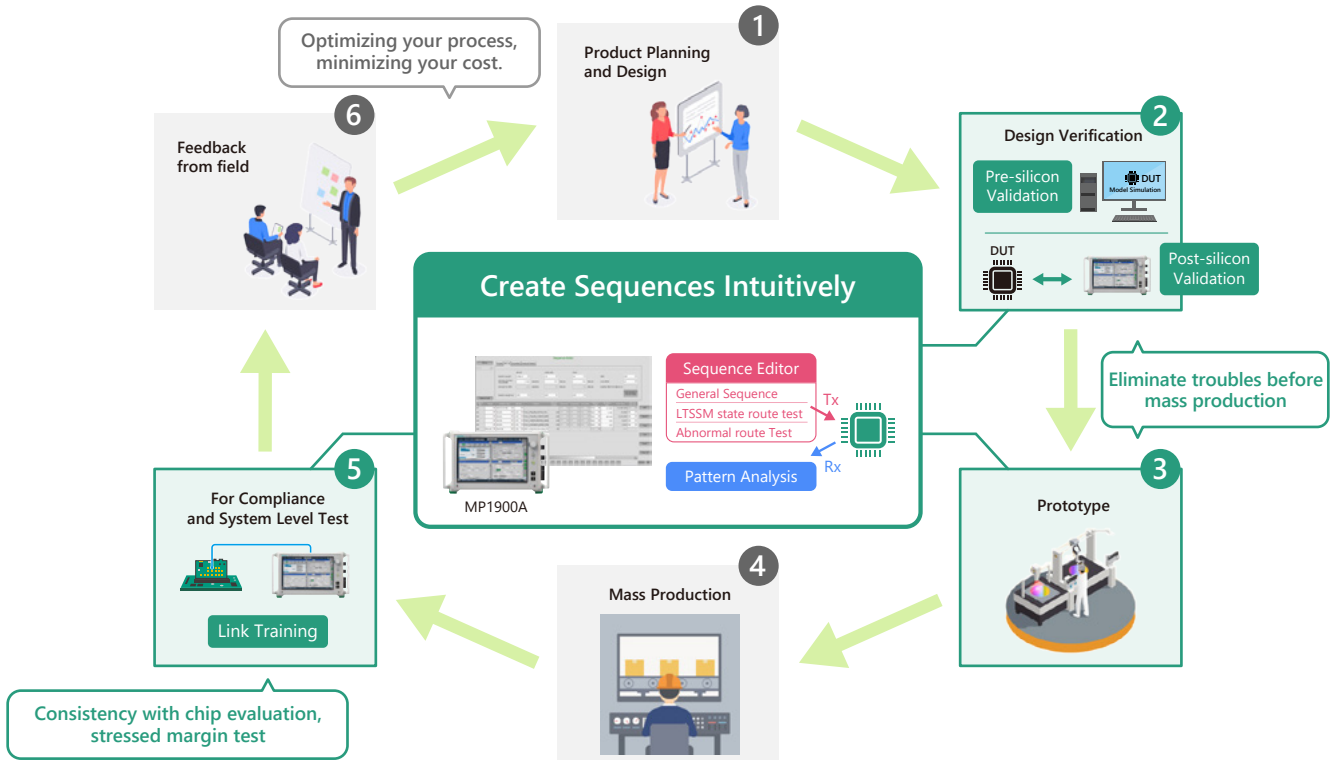
### Reproduce Real-World Usage Environments using Sequence Editor to Facilitate Early Resolution of Potential Issues

#### Addressing High-Speed Bitrate Issues

Increasing bit-rate speeds make differentiating between physical layer errors and protocol errors more complex, which increases the burden of verification and debugging. Sequence Editor helps speed-up debugging by analyzing and isolating these errors efficiently.

#### Solving Challenges Beyond Compliance Testing in Multi-Channel Environments

By supporting not only 1 Lane but also 2- and 4-Lane configurations, Sequence Editor can reproduce both Compliance Test environments as well as actual market usage environments. This enables identification and resolution of potential issues in advance by reproducing load conditions according to real-world usage environments, thereby mitigating troubles after product launch.

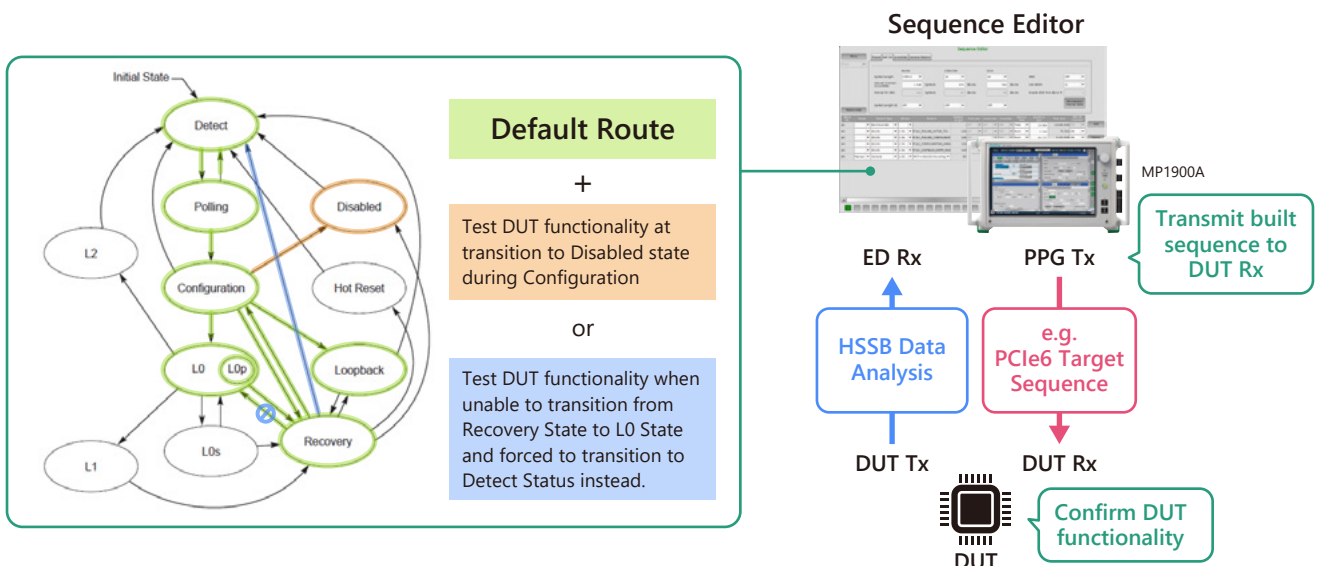


### User-Friendly Sequence Editor Supporting PCIe 1 to 6 and USB 3.2, with HSSB Data Analysis Function

#### Transmission Pattern Customization and Advanced Debugging Support

Users can use the Sequence Editor function freely to create and edit transmission patterns for PCIe 1-6 and USB 3.2.

Users can reproduce actual Link Training behavior by using LTSSM logs and can debug Link Training easily by changing the conditions of states that are not operating normally. Data received from the DUT can be displayed easily using the HSSB Data Analysis function (SI ED only).



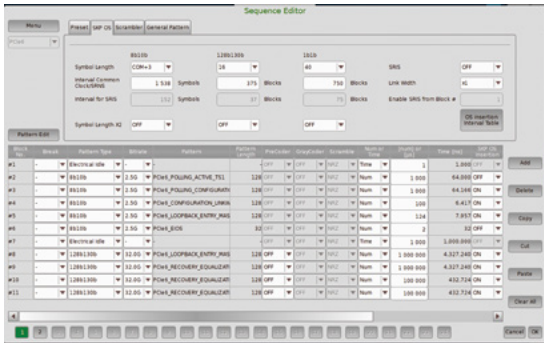
# Sequence Editor (PCIe1 to 6, USB3.2, Multi-channel) (cont'd)

## Intuitive and Excellent Usability

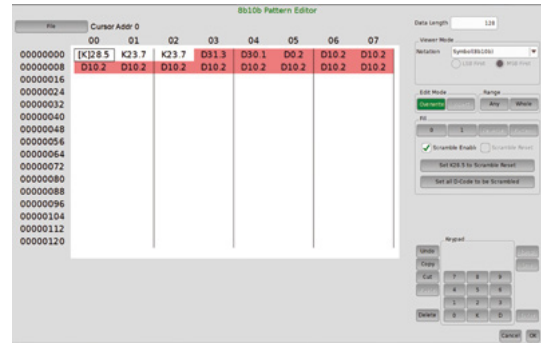
Sequence Editor features a dedicated user interface for PCIe 1 to 6 and USB 3.2, enabling intuitive sequence creation.

Both symbol-level editing for 8b/10b, 128b/130b, and 1b/1b, as well as scrambler settings for arbitrary symbols are easily configured.

The ability to customize ordered set information and transmission counts and sequences makes simplifies creation of test cases, significantly contributing to higher test quality and reproduction of bugs.



Sequence Editor Screen



8b/10b Pattern Editor Screen (Scrambled)

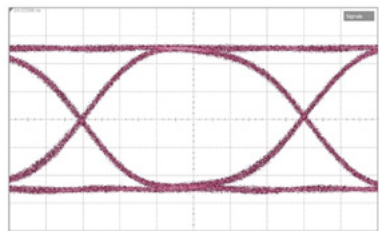
# SI PPG/ED High Waveform Quality and High Sensitivity

## Low-Noise, High-Quality BERT with Low Intrinsic Jitter Output, High Sensitivity and Wideband Input

Assuring DUT design margins has become an important issue as transmission rates have become faster and PAM4 Signal formats have been introduced. Designers require more accurate evaluations to confirm that adequate margins are maintained. As a result, the impact of uncertainty elements, such as noise and Intrinsic Jitter characteristics of measuring instruments, on results can no longer be ignored. These newly developed best-of-class PPG with lowest-level Intrinsic Jitter and high-sensitivity ED can measure DUT guaranteed margins more accurately to help improve R&D efficiency.

### Low Intrinsic Jitter Data Output PPG

The MU195020A PPG has an Intrinsic Jitter of just 115 fs rms.



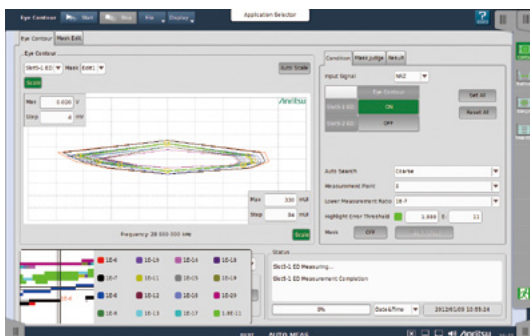
28.1 Gbit/s PRBS  $2^{31} - 1$   
Typical Output Waveform



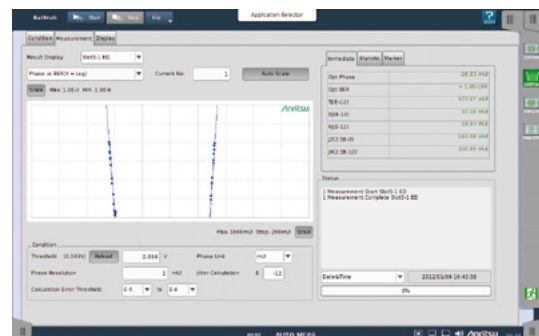
Low intrinsic RJ 115 fs rms

### High-Sensitivity, Wideband Input ED

The assured ED input analog bandwidth is 40 GHz. This bandwidth supports evaluation of Eye margin characteristics with high reproducibility even at input of small signals.



Example of Eye Contour Measurement at Input of Small 50 mVp-p Signal



Bathtub Measurement Example

# PCIe Compliance Test

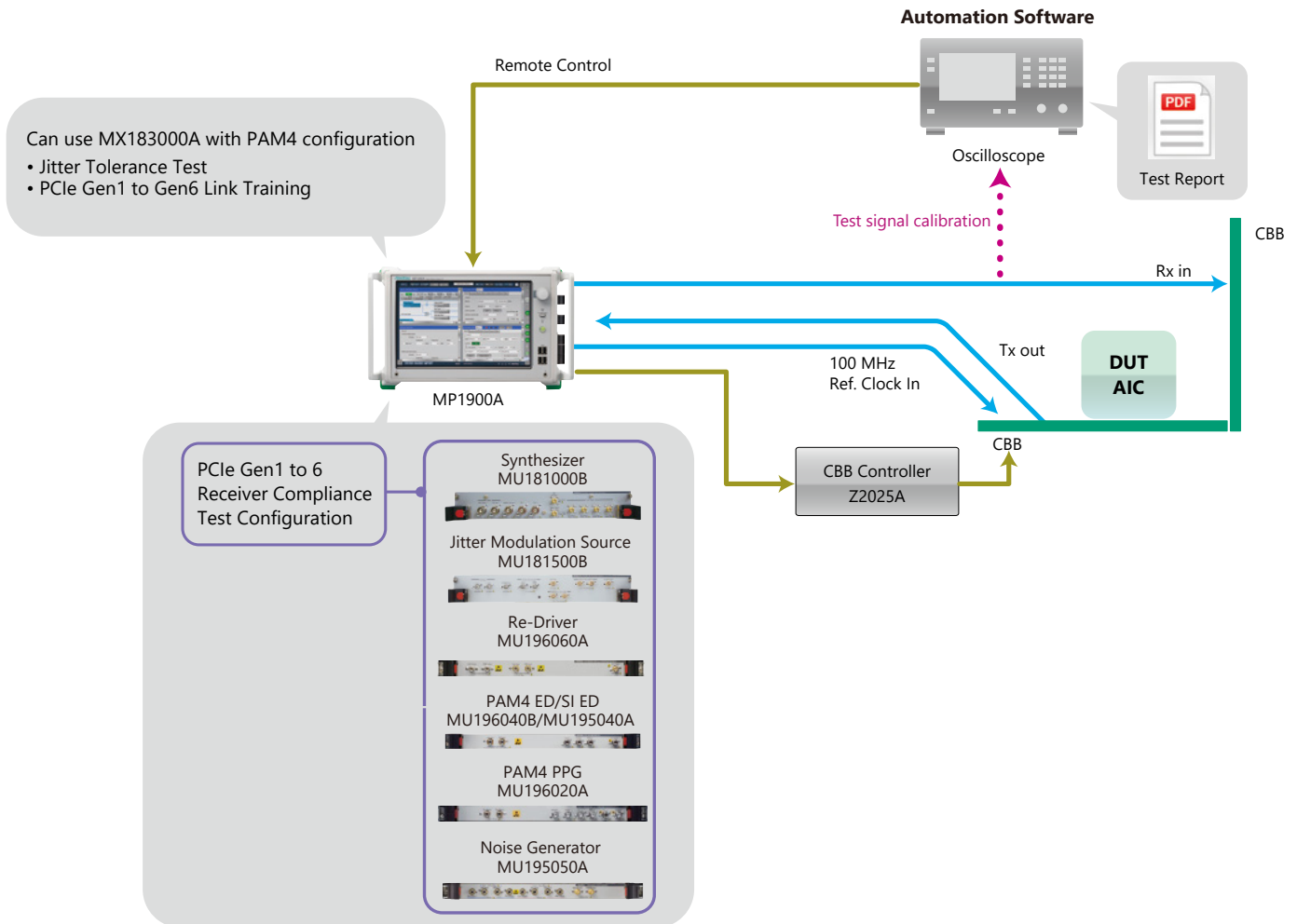
The PCIe Gen6 standard uses PAM4 coding. Although the transmission efficiency is double that per clock compared to NRZ, PAM4 has an increased signal error rate due to the 9.5 dB degraded signal to noise ratio (SNR) caused by the lower amplitude level of each Eye.

As a result, test instruments for measuring PAM4 must generate high-quality signals and require a high receiver sensitivity and an equalizer function.

With industry-beating signal integrity and high sensitivity, the MP1900A PAM4 supports improved wideband measurement efficiency.

The all-in-one MP1900A with installed PAM4 PPG/ED and SI ED modules is the ideal solution for PCIe Gen1 to Gen6 Link Training and stress tests.

Contact our business section about support for PCIe Gen6 compliance test.

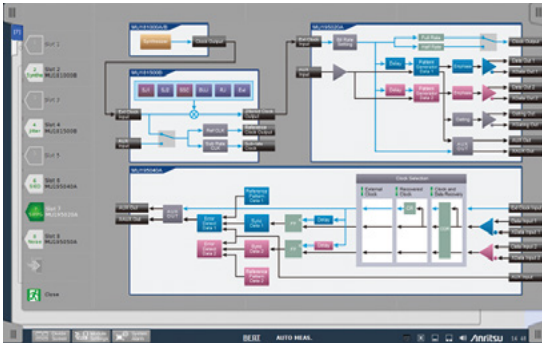


# Easy to Use Operability

## Improved Operability with New System View, User Interface, and Multi-windows

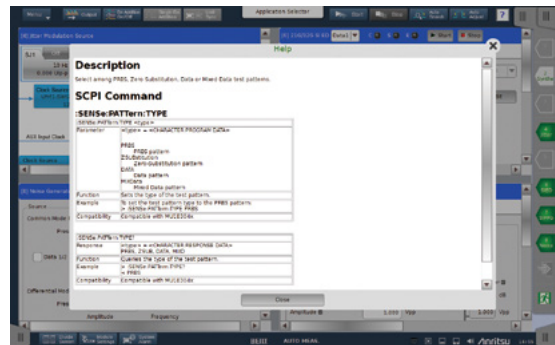
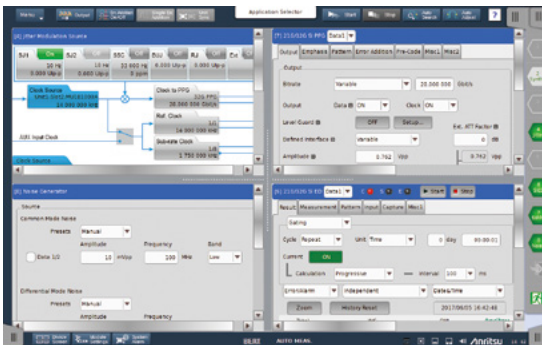
The MP1900A features easy intuitive operability based on a redesigned GUI and large 12.1-inch touch-panel LCD. Fast mistake-free settings help shorten measurement times.

The newly developed system view displays system functions as easy-to-understand blocks, supporting smooth settings and easy operation of each module.



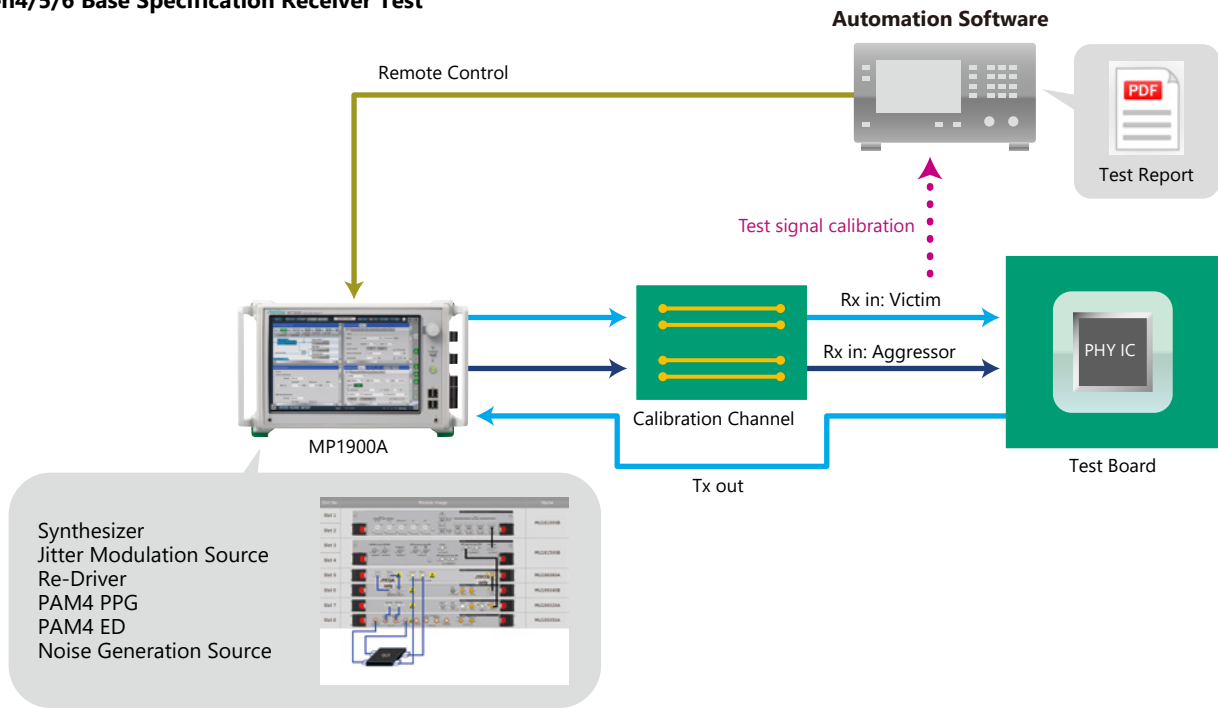
Four split screens help improve the efficiency of multi-channel measurements.

The Help function displays the remote commands corresponding to GUI operations, which simplifies automated system configurations.



# Application Examples

## PCIe Gen4/5/6 Base Specification Receiver Test



### Required Items

- Jitter Tolerance Test
- Emphasis Effect Validation
- Supports Common/Separate Clock Architecture

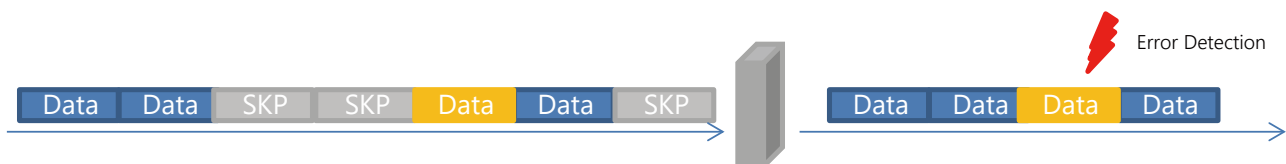
## PCI Express Gen6 Base Solution Features

- True BER Measurement using SKP OS Filtering Function
- Support for All SRIS, SRNS, and Common Clock Architectures
- Support for FEC Uncorrectable Error Real-time Measurement

### SKP OS Filtering

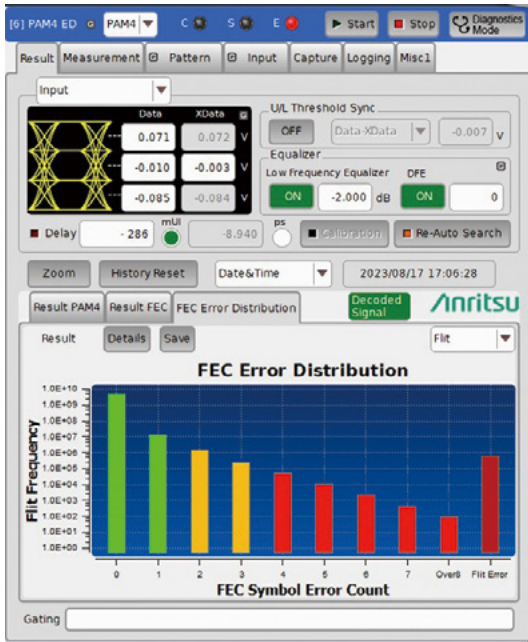
The SKP Symbol used to absorb frequency deviation must be excluded from the target BER measurement. The Error Detector automatically discriminates between Data and SKIP symbols to measure the true BER.

This function supports PCIe Gen1 to Gen5.



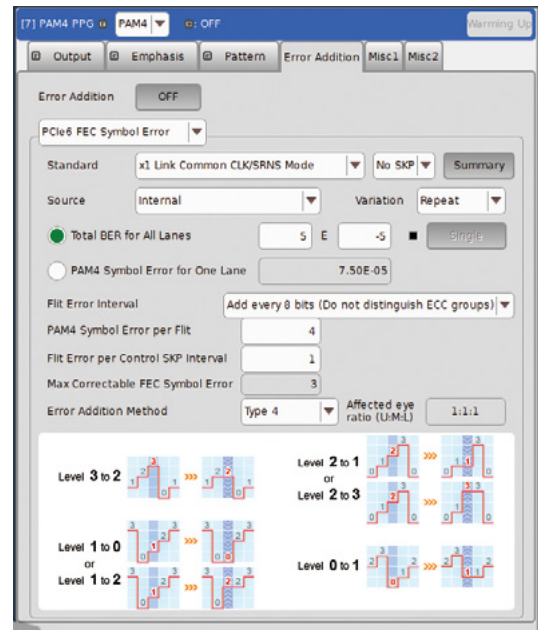
## Real-time measurement of FEC Uncorrectable errors

FEC Error Distribution function for measurement and real-time display of correctable and uncorrectable errors. This allows accurate evaluation of the correction capability by FEC even at receiver tests with FBER (First Bit Error Rate) 1E-6 threshold.



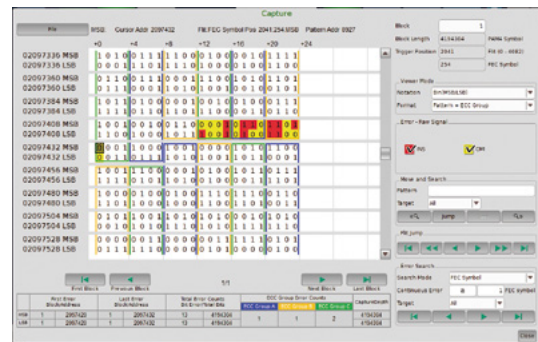
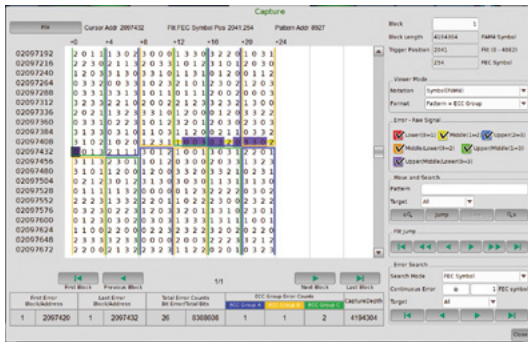
## Supports verification of DUT error correction capability using error addition

PPG Error Addition function to add various types of error to FLIT (Flow Control Unit) data, helping verify the DUT FEC capability under stress conditions.



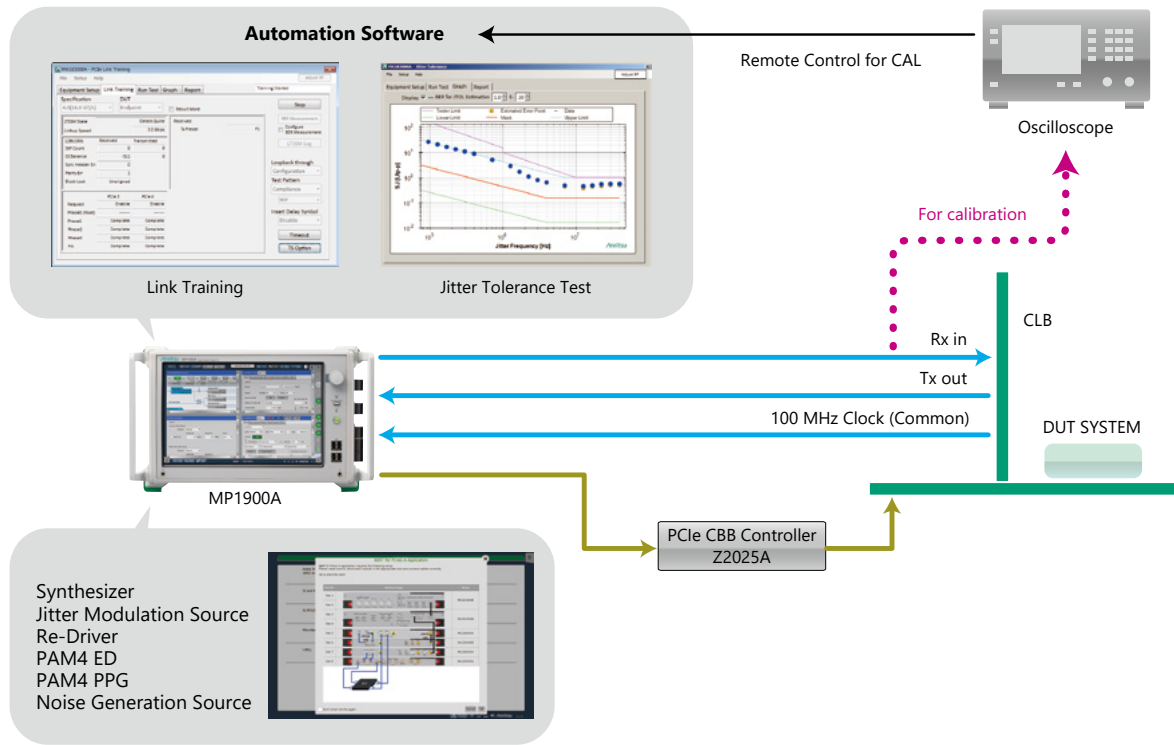
## FEC Capture

FEC Capture function to capture Burst and other errors causing FLIT loss, supporting analysis of infrequent system failures and identification of cause, which can be time-consuming otherwise.



# Application Examples

## PCIe Gen4/5/6 CEM Specification Receiver Test



### Video

- [PCIe 6.0 Compliance Test](#)
- [PN Skew Evaluation Solution Demonstration Video](#)
- [PCIe® 6.0 RxLEQ Tests Demonstration Video](#)

### Required Items

- Link Training function
- Jitter Tolerance Test
- Emphasis Effect Validation
- Supports Common/Separate Clock Architecture

### PCI Express CEM Solution Features

- All-in-one support for Protocol Awareness PCIe Gen1 to Gen6 receiver tests
- Event Trigger Function for Tx/Rx Link Equalization Test
- 64.2 Gbit/s (32.1 Gbaud, PAM4) high-speed BERT
- Low-intrinsic-jitter and high-quality output waveform, high-sensitivity ED
- Link Training, Link Equalization and LTSSM analysis functions
- 4Tap Emphasis function
- CTLE and Clock Recovery functions
- CMI and DMI Noise addition, and SJ, RJ, BUJ, and SSC Jitter Addition functions
- Full automation including CBB control

### PCIe CBB Controller Z2025A

The DUT must be reset and transitioned to the Initial state before starting Link Training.

The PCIe CBB Controller Z2025A fully automates control of Rx LEQ and Tx LEQ using the Power Reset and Power Cycle control pins implemented by PCIe CBB 4.0 (Compliance Base Board 4.0).

### PCIe Re-Driver MU196060A

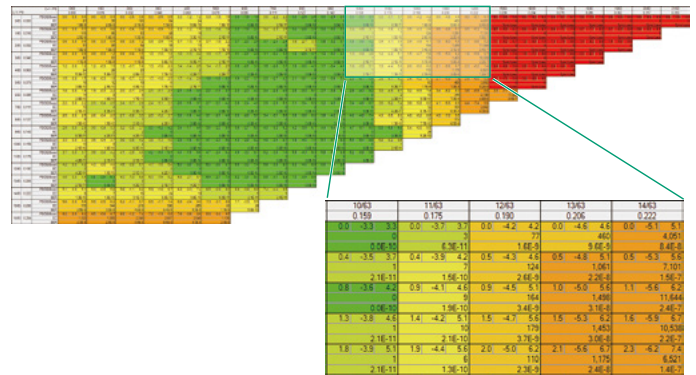
The Rx test requires establishment of a DUT return path. If the return-path physical loss is greater than about 18 dB (for PCIe5 NRZ), connection of an external equalizer is recommended since there is a risk of detecting errors in the return path.\*

The return path can be established by using MU196060A.

\*: The Re-Driver module (MU196060A) is required when using the PAM4 ED.

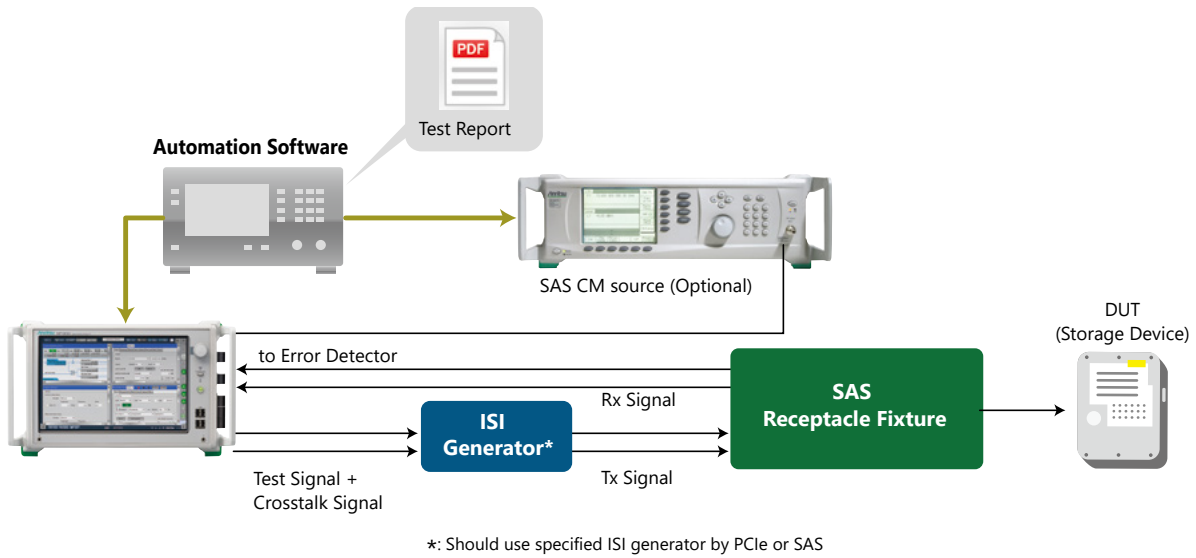
### Matrix Scan Function

To secure high-quality communications with the Link partner, the best combination of the Tx-side EQ and Rx-side EQ must be selected. The Matrix scan function scans for the best Tx EQ setting at the RX to find the best setting automatically at the receiver.



# Application Examples

## SAS-3/-4 Receiver Test



### Required Functions

- 12 Gbit/s to 22.5 Gbit/s BERTS
- Stressed Signal Calibration and Test
- Jitter Margin Test

### Wideband BERTS

The same configuration covers SAS-3 (12 Gbit/s), SAS-4 (22.5 Gbit/s) and PCI Gen1 to Gen5 measurements.

### Receiver Test

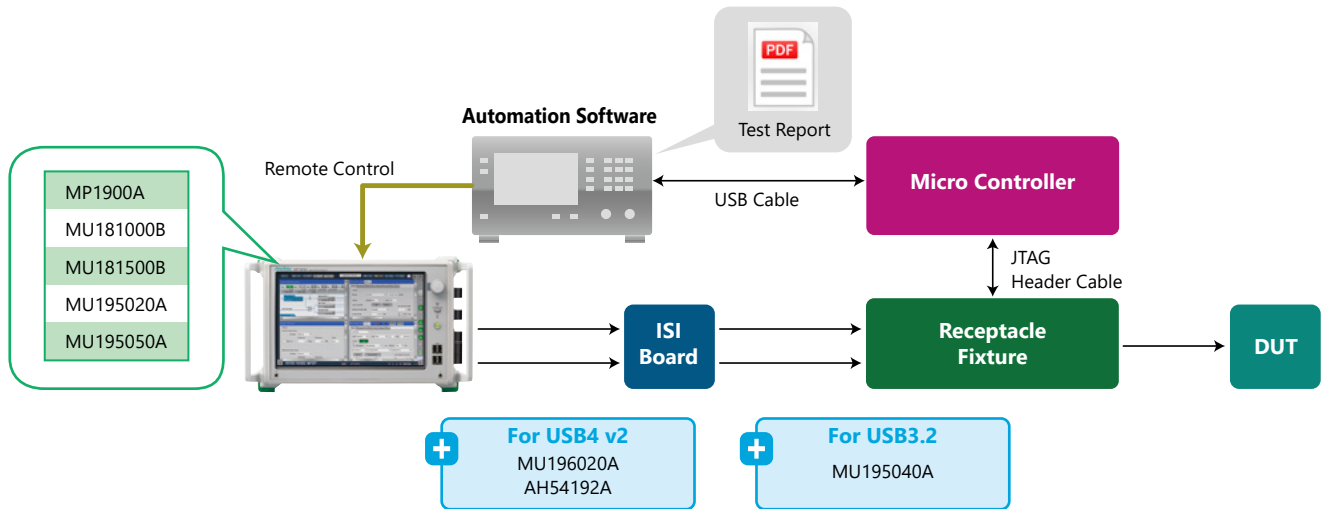
Stressed signal calibration and measurements can be automated using the automation software to shorten the design stage by cutting Compliance test times and improving measurement reproducibility.

### Jitter Margin Test

The automation software supporting jitter tolerance tests helps simplify receiver performance evaluations required by storage, HBAs, and ICs.

# Application Examples

## USB4 v1, v2, Thunderbolt3/4 Receiver Test



### Required Functions (USB4 v1, Thunderbolt3/4)

- 20 Gbit/s PPG
- Stressed Signal Calibration Function
- Jitter Tolerance Function

### Required Functions (USB4 v2)

- USB4 v2 25.6 Gbaud (NRZ/PAM3)
- Stressed Signal Calibration Function
- Frequency Variation Profile Function

### Supports USB Type-C

Supports specified bit rates.

USB4 v1 (NRZ)	20 Gbaud
USB4 v2 (NRZ/PAM3)	25.6 Gbaud
Thunderbolt3/4	20.625 Gbaud

### Stressed Signal Calibration

Automation Software supports automatic stressed signal calibration as specified by USB Type-C.

### Stressed Signal Input Test

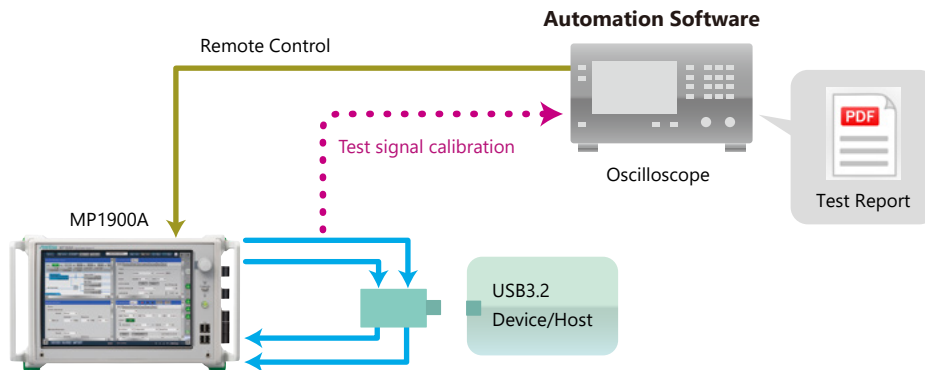
- Supports Rx BER measurements required by Host/Device compliance test
- Supports automatic Rx test using Tenlira scripts
- Supports automatic Pass/Fail measurement for Rx stressed signal tests

### Receiver Test

Calibration, TER test (USB4 v2) and BER test (USB4 v1, Thunderbolt3/4) can both be automated using the automation software. Automation helps cut design verification times.

# Application Examples

## USB 3.2 Gen1/2 Receiver Test



### Required Functions

- Loopback State Setting Function
- Jitter Tolerance Function
- Automatic Receiver Test Function
- Link Training Function

### Link Training Function

Automated evaluation of BER required by the Compliance Test can be configured using the MX183000A and MX183000A-PL022/023 option.

- Supports transition to Loopback mode used for USB 3.2 Gen1/2 ×1 and ×2 device evaluation
- Supports troubleshooting using LTSSM analysis function when unable to transition to Loopback mode
- Detailed troubleshooting analysis is supported by changing the timeout for each state
- Supports easy troubleshooting when problems occur when changing timeout at each state by using LTSSM trigger to capture transient signals using oscilloscope when state does not transition normally

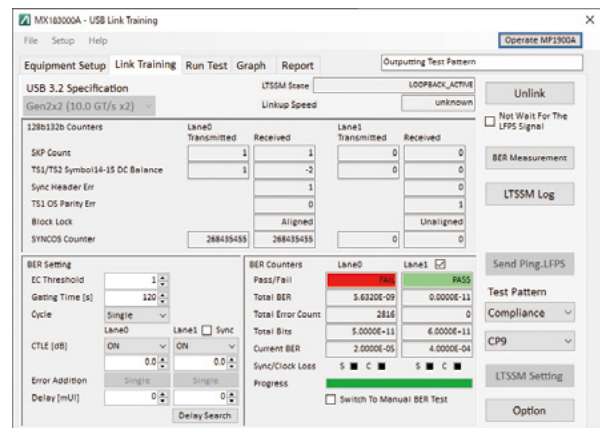
### Receiver Jitter Tolerance Test

Jitter Tolerance tests can be automated using the MX183000A-PL001 software to help shorten the design validation time.

### x2 Device Evaluation

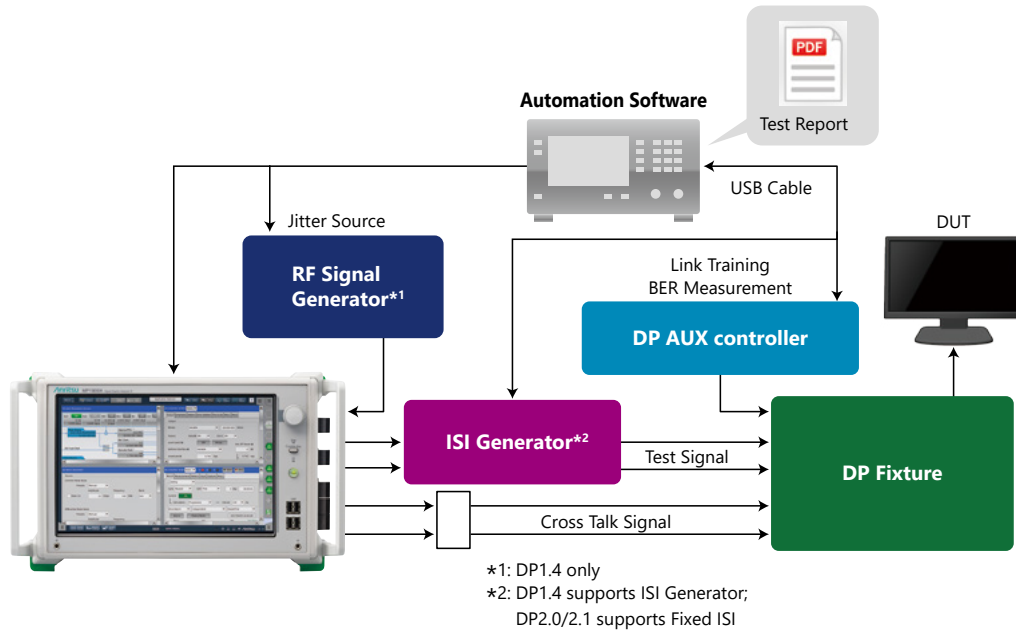
Lane 0 and Lane 1×2 devices can be evaluated simultaneously using the MX183000A-PL023.

Crosstalk effects can also be analyzed by impressing skew between lanes.



# Application Examples

## DisplayPort 1.4/2.0/2.1 Sink Test



### Required Functions

- 2.7 Gbit/s to 20 Gbit/s PPG
- Stressed Signal Calibration and Test
- USB Type-C Alternative Mode Operation

### Wideband PPG

One module covers RBR (1.62 Gbit/s)\*, HBR (2.7 Gbit/s), HBR2 (5.4 Gbit/s), HBR3 (8.1 Gbit/s), UHBR10 (10 Gbit/s), UHBR13.5 (13.5 Gbit/s), and UHBR20 (20 Gbit/s).

Expandable up to 32 Gbit/s without hardware upgrade.

\*: Can generate special RBR (1.62 Gbit/s) pattern

### Sync Sensitivity Test

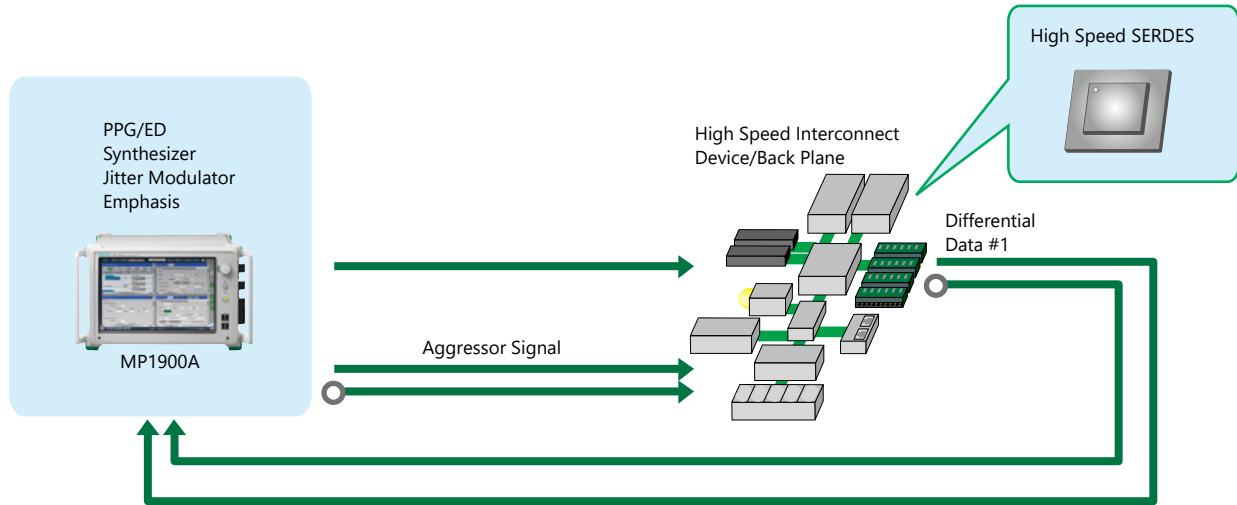
Stressed signal calibration and measurements can be automated using the automation software to shorten the design stage by cutting Compliance and Jitter Tolerance Margin test times and improving measurement reproducibility.

### USB Type-C Alternative Mode

Measurement of the Alternative Mode transmitting Display Port signals using the Auto USB Type-C connector is supported.

# Application Examples

## High-speed Interconnect Evaluation



### Required Test Items

- 32.1 Gbit/s Multi-channel signal generation
- Jitter Tolerance test
- Emphasis efficiency check
- Crosstalk test

### Multi-channel

Along with support for multi-channels, the bit rate of devices such as back planes of high-performance servers is becoming increasingly faster. The MP1900A supports generating both the Victim signal with controlling Emphasis and the Aggressor signal for crosstalk testing simultaneously. The MP1900A offers multi-channel measurements for TRx devices such as Transceiver, SERDES and Clock Data Recovery (CDR).

### Skew and Crosstalk Effect Check

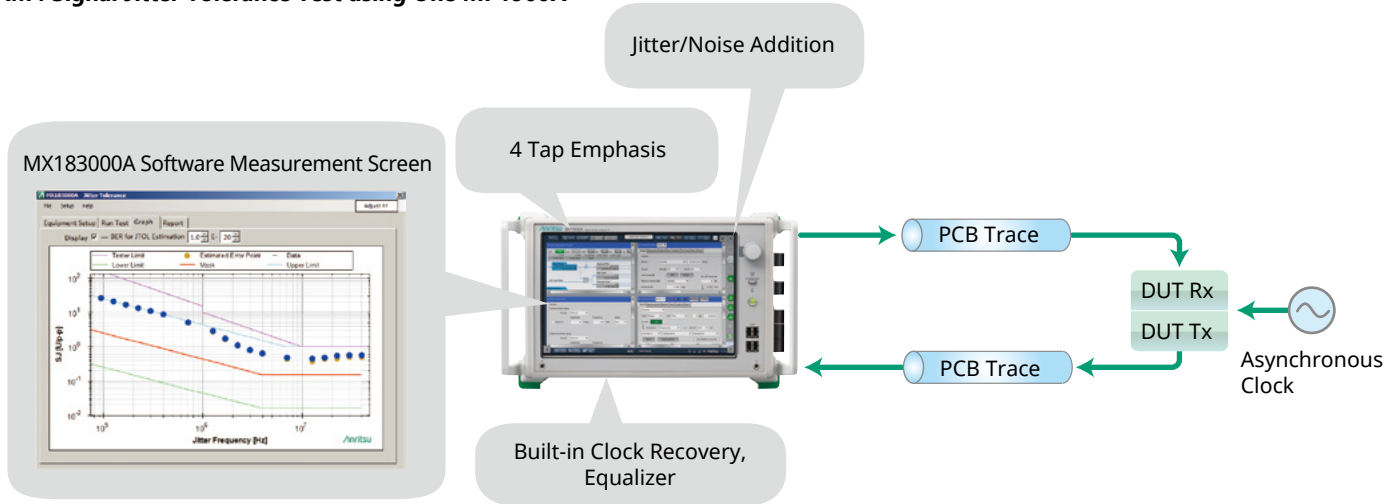
Processing high speed digital signals requires both logic tests and actual equipment tests. The MP1900A supports both pattern synchronization and phase adjustment functions, permitting easy tests of Rx device skew tolerance and crosstalk effects.

### Jitter Tolerance Test

Jitter Tolerance tests supporting various standards can be run by simultaneously impressing SJ (2 tone), RJ, BUJ, and SSC up to 32.1 Gbit/s using the MX183000A-PL001 and MU185000B Jitter modulation sources. The Eye opening of signals passing through the back-plane is degraded by loss in the board traces.

# Application Examples

## PAM4 Signal Jitter Tolerance Test using One MP1900A



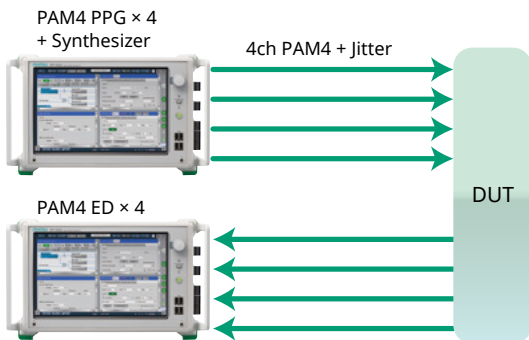
### Required Items

- PAM4 BER measurement
- Jitter Tolerance Test

### BER Measurements of 64-Gbaud PAM4 Signals

BER measurements can be performed in real-time using the PAM4 PPG and ED modules with no need for other external equipment\*.

- All in one solution requiring no other external equipment
- Module with built-in clock recovery, equalizer
- Wide-range Emphasis function
- High-sensitivity data input
- Symbol BER evaluation



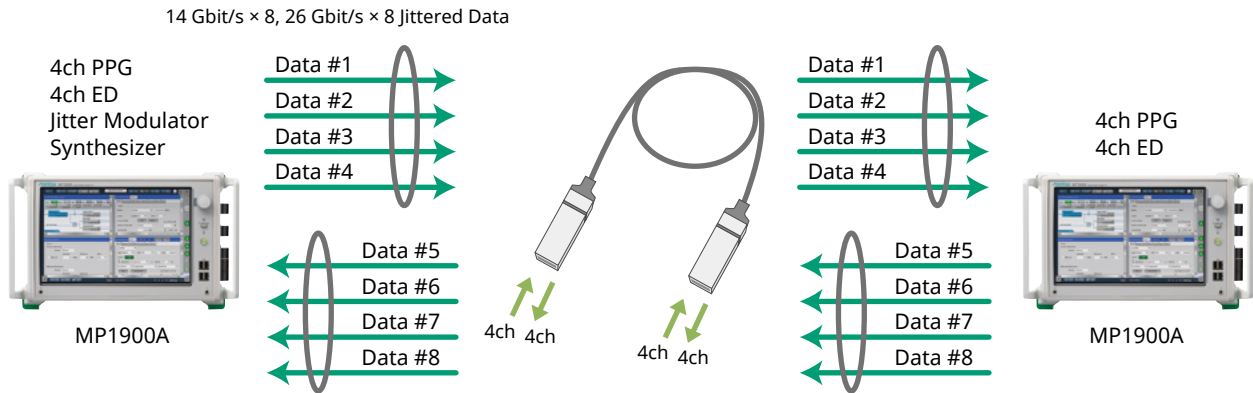
\*: Refer to the 32G/64G NRZ/PAM4 Signal Integrity Test Solution Catalog (MP1900A\_64G-E-A-1) for details of PAM4 PPG/ED.

### Jitter Tolerance Test

Testing the DUT receiver input stress tolerance requires BER measurements under severe conditions using a stressed signal with added jitter and noise. The all-in-one MP1900A series supports receiver stress tests for various interface specifications using the Jitter Modulation Source MU181500B for adding SJ, RJ, BUJ, and SSC simultaneously, the Jitter Tolerance Test MX183000A-PL001 software, and the Noise Generator MU195050A for adding CM/DM/White voltage noise. The MP1900A series provides strong support for high-quality signals prior to jitter and noise addition, as well as receiver stressed-signal tolerance tests using high-linearity jitter and noise addition functions.

# Application Examples

## InfiniBand EDR (25.78G) AOC Evaluation



### Required Test Items

- 8ch (4ch two ways) simultaneous BER measurement
- Crosstalk Test
- Jitter Tolerance Test
- Bathtub Jitter and Eye Diagram Analysis

### 8ch (4ch two ways) Simultaneous BER Measurement

The MP1900A supports up to eight PPG or ED channels simultaneously using SI PPG/ED modules. Additionally, up to four PPG or ED channels are supported simultaneously in one chassis using PAM4 PPG/ED modules.

QSFP Active Optical Cables (AOC) used by InfiniBand, etc., perform simultaneous transmission over a total of 8 channels using two-way transmissions over 4 channels. The MP1900A can incorporate up to 8 channels simultaneously in one main unit and can measure all channels at one time, offering excellent performance and shorter measurement times. Moreover, InfiniBand HDR measurement is also supported using PAM signals.

### Jitter Tolerance Test

AOCs in data centers are using low input and output amplitude levels to cut power consumption costs, making it important to assure interconnectivity. With its high sensitivity data input and CTLE, the MU195040A supports reception of low-amplitude, low-Eye-opening Data signals and perform high-reproducibility DUT Jitter Tolerance tests.

### Crosstalk Effect Confirmation

Implementing 20 Gbit/s class transmissions not only requires logic tests but also requires actual equipment verification tests. Since the MP1900A has both pattern synchronization and independent phase tuning for each channel, tests on items such as the effect of AOC crosstalk are implemented easily.

### Bathtub Jitter and Eye Diagram Analysis

Bathtub Jitter Analysis (separate TJ, RJ, DJ) is supported by the built-in as standard Clock Delay function. Low bit error rates, such as 1E-12 and 1E-15, can also be estimated quickly from the change in bit error rate versus phase.

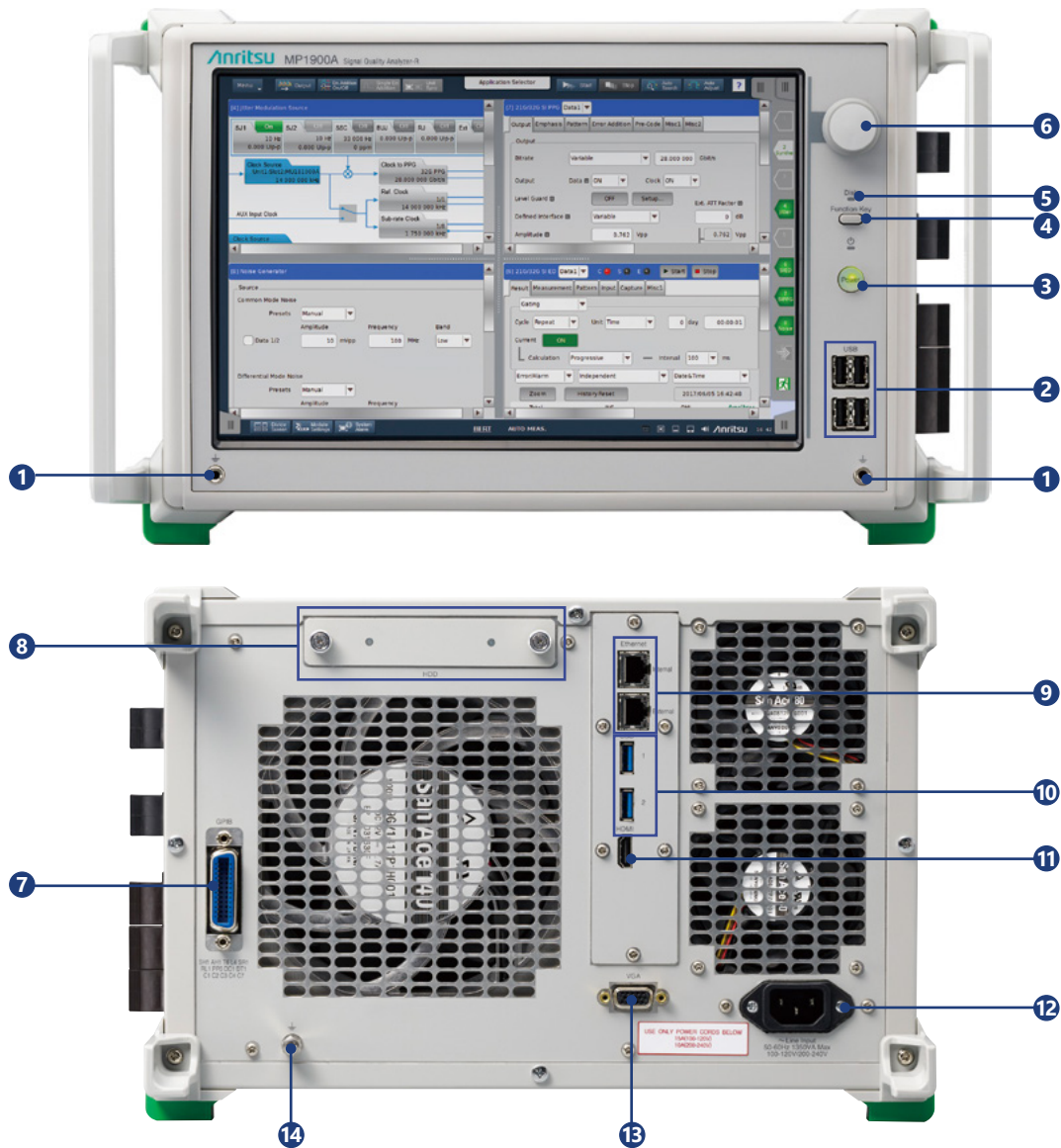
## Automation Software Selection Guide

The MP1900A can execute the following receiver tests using automation software in combination with a real-time oscilloscope. Refer to the next page for option configurations required by the MP1900A. Refer to the Selection Guide (MP1900A-E-Z-1) for the supported combination of real-time oscilloscopes and automation software.

Interface Type	Compliance Test Item	
PCIe Gen 3/4/5/6	Base Spec	Stressed Eye Test
	CEM Spec	Transmitter initial Tx Equalization Transmitter Link Equalization response (Tx LEQ) Receiver Link Equalization (Rx LEQ) PLL Bandwidth
USB3.2 Gen1/2	Transmitted Eye Test Receiver Jitter Tolerance Test	
USB Type-C (USB4, Thunderbolt3/4)	Receiver Test SJ Margin Test Amplitude Margin Test	
SAS-3/-4	Receiver Jitter Tolerance Test	
DP1.4/2.0/2.1	Sink Jitter Tolerance Test	

# Signal Quality Analyzer-R MP1900A Panel Layout

## Front/Rear Panel

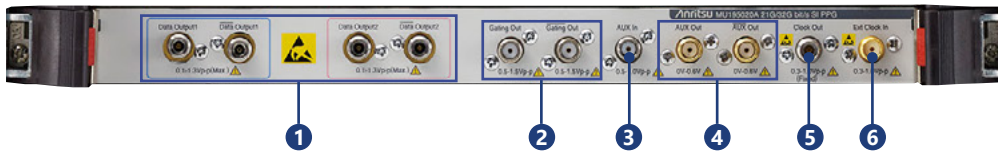


- 1 Ground Jack**  
Wrist strap to discharge static electricity
- 2 USB Port**  
Four USB2 ports for connecting peripherals
- 3 Power Switch**  
Switches power on and off; Standby LED over power switch lights when power cord connected and Power switch set to off
- 4 Function Keys**  
Keys for defining functions using software
- 5 HDD Access LED**  
Lamp that lights during access to built-in HDD
- 6 Rotary Encoder**  
Switch to increase/decrease numeric values by turning knob
- 7 GPIB**  
GPIB Connector
- 8 HDD**  
Slot for secondary 2.5" HDD
- 9 Ethernet Connector**  
External: For Remote Control  
(Internal: Reserved for future function expansion)
- 10 USB Port**  
Two USB3.0 ports for peripherals
- 11 HDMI**  
HDMI connector for displaying screens on external screen
- 12 Power Inlet**  
Socket for connecting 3-pole power cord to supply 100 V(ac) to 12 V(ac) or 200 V(ac) to 240 V(ac) power
- 13 VGA**  
VGA connector for displaying screens on external screen
- 14 Frame Ground Terminal**  
Terminal for discharging electrostatic charges; connect DUT and common ground using ground strap

# Signal Quality Analyzer-R MP1900A Panel Layout

## Modules

### 21G/32G bit/s SI PPG MU195020A



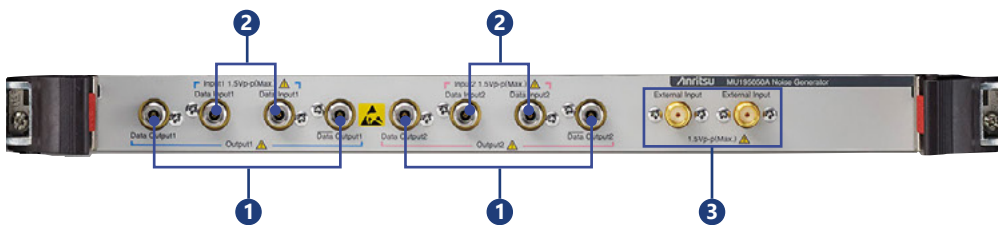
- 1 Data Output, Data Output**  
Connectors outputting differential Data and  $\overline{\text{Data}}$  signals
- 2 Gating Out, Gating Out**  
Repeat: Timing signal output  
Burst: Timing signal output used at Burst
- 3 Aux In**  
Auxiliary signal input connector  
Either Error Injection or Burst can be selected.
- 4 Aux Out, Aux Out**  
Auxiliary signal output connectors  
Output of any of 1/N Clock, Pattern Sync, and Burst2 can be selected.
- 5 Clock Out**  
Clock signal output connector
- 6 Ext Clock In**  
Clock signal input connector

### 21G/32G bit/s SI ED MU195040A



- 1 Data Input, Data Input**  
Input connectors for Data and  $\overline{\text{Data}}$  signals  
Supports both differential and single inputs  
When the Clock Recovery MU195040A-x22 is installed, the clock is recovered from the signal input to Data Input1.
- 2 Aux In**  
Auxiliary signal input connector  
Any of External Mask, Burst, and Capture External Trigger can be selected.
- 3 Aux Out, Aux Out**  
Auxiliary signal output connectors  
Any of 1/N Clock, Pattern Sync, Error, Sync Gain can be output.
- 4 Ext Clock In**  
Clock signal input connector

### Noise Generator MU195050A



- 1 Data Output, Data Output**  
Connector for outputting differential Data and  $\overline{\text{Data}}$  Signal with added noise
- 2 Data Input, Data Input**  
Connector for inputting Data and Data signal with added noise
- 3 External Input, External Input**  
External noise input connectors

\* Input2 and Output2 are not used by the MU196020A

# Signal Quality Analyzer-R MP1900A Panel Layout

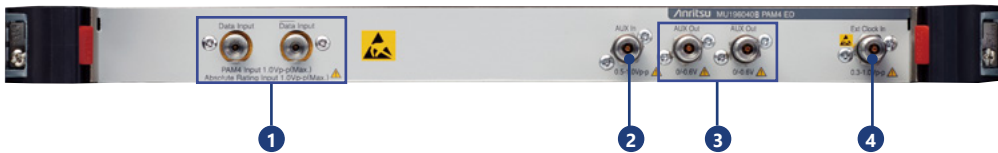
## Modules

### PAM4 PPG MU196020A



- 1 Data Output,  $\overline{\text{Data}}$  Output**  
Connectors outputting differential Data and  $\overline{\text{Data}}$  signals
- 2 Gating Out**  
Repeat: Timing signal output  
Burst: Timing signal output used at Burst
- 3 Aux In**  
Auxiliary signal input connector  
Either Error Injection or Burst can be selected.
- 4 Aux Out,  $\overline{\text{Aux}}$  Out**  
Auxiliary signal output connectors  
Output of any of 1/N Clock, Pattern Sync, and Burst2 can be selected.
- 5 Clock Out**  
Clock signal output connector
- 6 Ext Clock In**  
Clock signal input connector

### PAM4 ED MU196040B



- 1 Data Input,  $\overline{\text{Data}}$  Input**  
Input connectors for Data and  $\overline{\text{Data}}$  signals  
Supports both differential and single inputs
- 2 Aux In**  
Auxiliary signal input connector  
Any of External Mask, Burst, and Capture External Trigger can be selected.
- 3 Aux Out,  $\overline{\text{Aux}}$  Out**  
Auxiliary signal output connectors  
Any of 1/N Clock, Pattern Sync, Error, Sync Gain can be output.
- 4 Ext Clock In**  
Clock signal input connector

### 32G baud NRZ/PAM4 Re-Driver MU196060A

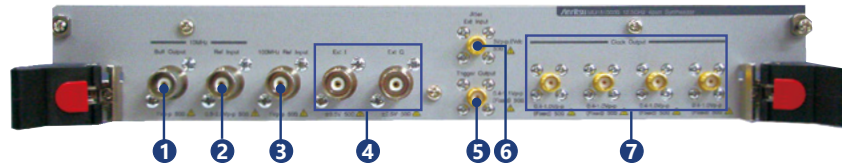


- 1 Data Output,  $\overline{\text{Data}}$  Output**  
Connectors for outputting equalized differential Data and  $\overline{\text{Data}}$  signals
- 2 Data Input,  $\overline{\text{Data}}$  Input**  
Connectors for inputting differential Data and  $\overline{\text{Data}}$  signals
- 3 Clock Output**  
Connector for outputting Clock signal recovered from input data

# Signal Quality Analyzer-R MP1900A Panel Layout

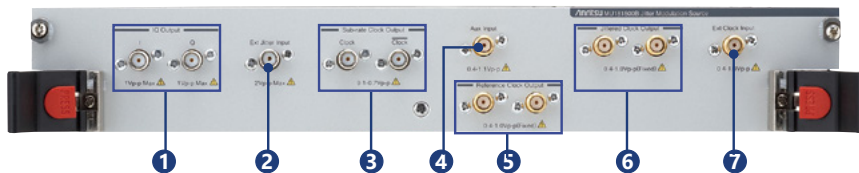
## Modules

### 12.5 GHz 4port Synthesizer MU181000B



- 1 10 MHz Buff Output**  
Output 10 MHz clock for reference
  - 2 10 MHz Ref Input**  
Inputs 10 MHz clock for reference
  - 3 100 MHz Ref Input\*1**  
Inputs 100 MHz clock for reference
  - 4 Ext I, Q\*2**  
Inputs I, Q signals
  - 5 Trigger Output\*2**  
Outputs 1/1 or 1/64 clock frequency
  - 6 Jitter Ext Input\*2**  
Inputs modulation signal source
  - 7 Clock Output 1 to 4**  
Outputs clocks
- \*1: Only when Jitter Modulation Option (MU181000B-001) or SSC Extension (MU181000B-002) installed  
\*2: Only when Jitter Modulation Option installed (MU181000B-001)

### Jitter Modulation Source MU181500B



- 1 IQ Output**  
Outputs IQ signal
- 2 Ext Jitter Input**  
Inputs Jitter Modulation Source
- 3 Sub-rate Clock Output**  
Differential Clock Output signal generated from 1/8 to 1/256-divided Clock Output based on any of following Clock inputs  
• Ext Clock Input • Aux Input
- 4 Aux Input**  
Inputs clock signal
- 5 Reference Clock Output**  
Dual-system Clock Output signal generated from either 1/1, 1/2, or 1/4-divided Jitter Clock Output based on any of following Clock inputs  
• Ext Clock Input • Aux Input
- 6 Jittered Clock Output**  
Two outputs jitter modulated clock signal
- 7 Ext Clock Input**  
Inputs external clock

### 28G/32G bit/s PPG (1ch or 2ch) MU183020A



- 1 Data1/Data1 Output\*3**  
Output for 1ch differential data signal
  - 2 Data2/Data2 Output\*4**  
Output for 2ch differential data signal
  - 3 Gating Output**  
Output for burst timing signal
  - 4 Aux Input**  
Input for auxiliary signal
  - 5 Aux/Aux Output**  
Output for differential auxiliary signal
  - 6 Clock Output**  
Output for clock signal
  - 7 Ext Clock Input**  
Input for external clock signal
- \*3: Data/Data when 1ch option was selected.  
\*4: Not implemented when 1ch option was selected.

### 28G/32G bit/s High Sensitivity ED (1ch or 2ch) MU183040B



- 1 Data1/Data1 Input\*5**  
Input for 1ch differential data signal
  - 2 Data2/Data2 Input\*6**  
Input for 2ch differential data signal
  - 3 Aux Input**  
Input for auxiliary signal
  - 4 Aux/Aux Output**  
Output for differential auxiliary signal
  - 5 Ext Clock Input**  
Input for external clock signal
- \*5: Data/Data when 1ch option was selected.  
\*6: Not implemented when 1ch option was selected.

# Signal Quality Analyzer-R MP1900A Specifications

Refer to the MP1900A Data Sheet (MP1900A\_Datasheet-E-A-1) for detailed specifications.

## Signal Quality Analyzer-R MP1900A

LCD	12.1" WXGA 1280 × 800	
Remote Interface	GPIB, LAN	
Module Slots	8	
External Equipment Interface	USB × 6, VGA × 1, HDMI × 1	
OS	Window Embedded Standard 7	
Power Supply	100 V(ac) to 120 V(ac), 200 V(ac) to 240 V(ac), 50 Hz to 60 Hz Power consumption: 1350 VA max.	
Dimensions and Mass	340 (W) × 222.5 (H) × 451 (D) mm, 20 kg (excluding modules)	
CE	EMC	2014/30/EU, EN61326-1, EN61000-3-2
	LVD	2014/35/EU, EN61010-1
	RoHS	2011/65/EU, (EU) 2015/863, EN IEC 63000:2018
UKCA	EMC	S.I. 2016 No.1091, EN 61326-1, EN61000-3-2
	LVD	S.I. 2016 No.1101, EN 61010-1
	RoHS	S.I. 2012 No.3032, EN IEC 63000:2018

## 12.5 GHz 4 Port Synthesizer MU181000B

Clock Output	Number of Output: 4 Frequency Range: 0.1 GHz to 12.5 GHz, Steps: 1 kHz/1 MHz Level: 0.4 Vp-p to 1 Vp-p (AC) Connector: SMA (f), Termination: 50Ω/GND
10 MHz Input	Frequency: 10 MHz ± 10 ppm Level: 0.5 Vp-p to 2.0 Vp-p Connector: BNC, Termination: 50Ω/GND
10 MHz Output	Level: 1.0 Vp-p ± 30% (AC) Connector: BNC, Termination: 50Ω/GND
100 MHz Reference Signal Input (SSC Extension MU181000B-002)	Outputs either 100 MHz with phase deviation x25, x50, or x80 frequency-multiplied clock from Clock Output connector Supports PCI Express Host Refclk input Modulation Frequency: 30 kHz to 33 kHz Level: 0.15 Vp-p to 1.3 Vp-p (AC) Connector: BNC

## Jitter Modulation Source MU181500B

External Clock Input	Frequency Range: 0.800 000 GHz to 15.000 000 GHz Amplitude: 0.4 Vp-p to 1.0 Vp-p Connector: SMA (f), Termination: 50Ω/AC Coupling
Jittered Clock Output	Number of Output: 2 Amplitude: 0.4 Vp-p to 1.0 Vp-p Connector: SMA (f), Termination: 50Ω/AC Coupling
SJ1	Modulation Frequency: 10 Hz to 250 MHz Amplitude: 0 to 2000 UI @Modulation Frequency 10 kHz to 100 kHz 0 to 1 UI @Modulation Frequency 10 MHz to 250 MHz (Different depending on the operating bit rate)
Built-in SJ2	Modulation Frequency: 33 kHz, 87 MHz, 100 MHz, 210 MHz
Spread Spectrum Clocking (SSC)	Modulation Frequency: 28 kHz to 37 kHz Deviation: 0 to 7000 ppm
Random Jitter (RJ)	Bandwidth: 10 kHz to 1 GHz Amplitude: 0 to 0.5 UI (Different depending on the operating frequency)
Bounded Uncorrelated Jitter (BUJ)	PRBS Pattern Length: $2^n - 1$ ( $n = 7, 9, 11, 15, 23, \text{ or } 31$ ) BUJ Rate: 0.1 Gbit/s to 3.2 Gbit/s, 4.9 Gbit/s to 6.25 Gbit/s, 9.8 Gbit/s to 12.5 Gbit/s Filter Type (LPF 3 dB Bandwidth): 50, 100, 200, 300, 500 MHz, Through Amplitude: 0 to 0.5 UI (Different depending on the operating frequency)
External Jitter	Bandwidth: 10 kHz to 1 GHz

## Noise Generator MU195050A

Number of Channels	2
Insertion Loss	-3 dB
CMI: Common Mode Noise	0.1 GHz to 6 GHz: Sinusoidal wave
DMI: Differential Mode Noise	2 GHz to 10 GHz: Sinusoidal wave
White Noise	10 MHz to 10 GHz
Crest Factor	>5

# Signal Quality Analyzer-R MP1900A Specifications

Refer to the MP1900A Data Sheet (MP1900A\_Datasheet-E-A-1) for detailed specifications.

## 21G/32G bit/s SI PPG MU195020A

Operation Rate (NRZ)	2.4 Gbit/s to 21 Gbit/s or 32.1 Gbit/s
Number of Channels	1 or 2
Output Amplitude	0.1 Vp-p to 1.3 Vp-p (Single-end) 0.2 Vp-p to 2.6 Vp-p (Differential)
Emphasis	10Tap
Channel Emulator	Normal: Emulates Insertion Loss using S-parameter data Inverse: Performs De-Emphasis compensation for S-parameter Insertion Loss S-Parameter file: S2P,S4P
ISI	Emulates ISI output using CEI-28G/25G Nyquist frequency loss setting Supports loss control in combination with ISI Board J1758A accessory Insertion Loss setting: 1.5 to 25 dB, 0.01 dB step, Nyquist frequency 0 to 25 dB, 0.01 dB step, 1/2 Nyquist frequency
Tr/Tf (20 to 80%)	12 ps (typ.)
Random Jitter	115 fs rms (typ.)
PCIe, USB Link Training	Supported (MX183000A-PL021/PL022/PL025)
Output Connector	K (f)

## 21G/32G bit/s SI ED MU195040A

Operation Rate (NRZ)	2.4 Gbit/s to 21 Gbit/s or 32.1 Gbit/s
Number of Channels	1 or 2
Input Attitude	0.05 Vp-p to 1.0 Vp-p (Single-End) 0.1 Vp-p to 2.0 Vp-p (Differential)
Input Sensitivity (Eye Height)	15 mV (28.1 Gbit/s, NRZ) 30 mV/Eye (28.1 Gbaud, PRBS15, PAM4)
CTLE	Peak Frequency: 14, 8, 4 GHz Gain: 0 to -12 dB
Clock Recovery	Yes, supports SSC
PCIe, USB Link Training	Supported (MX183000A-PL021/PL022/PL025)
Input Connector	K (f)

## PAM4 PPG MU196020A

Operation Rate (PAM4/NRZ)	2.4 Gbaud to 32.1/58.2/64.2 Gbaud (option selection)
No. of Channels	1
Output Amplitude	70 mVp-p to 800 mVp-p (Single-end) 140 mVp-p to 1600 mVp-p (Differential)
Offset	-2 V to +3.3 V
Emphasis	4 Tap, -20 to +20 dB
Channel Emulator	Generates waveform with insertion loss and simulates waveform with corrected insertion loss Set by loading S-Parameter file (S2 P, S4 P)
ISI	Simulates ISI generation waveform Set using loss (-8.00 to 8.00 dB) at CEI-specified Nyquist frequency Used in combination with channel board, such as J1800A/J1758A (optional accessories parts), or Noise Module MU195050A
Independently Variable PAM4 3 Eye	20 to 50% (PAM4 Amplitude 0/3 level = 100%)
PAM4 Pattern	SSPRQ, PRBS13Q, PRBS31Q, RS-FEC, etc.
PAM4 Pattern Error Addition	MSB Error, LSB Error, LSB&MSB Error, RS-FEC Symbol Error, PCIe6 FEC Symbol Error
Tr/Tf (20 to 80%)	8.5 ps (typ., NRZ)
Random Jitter	170 fs rms (typ., NRZ)
Output Connector	V (f)

## PAM4 ED MU196040B

Operation Rates (PAM4/NRZ)	2.4 Gbaud to either 32.1 Gbaud, or 58.2 Gbaud (PAM4)/64.2 Gbaud (NRZ) (option selection)
No. of Channels	1
Input Amplitude	NRZ: $\leq 32.1G$ : 0.05 Vp-p to 1.0 Vp-p, $> 32.1G$ : 0.1 Vp-p to 1.0 Vp-p PAM4: $\leq 32.1G$ : 0.3 Vp-p to 1.0 Vp-p, $> 32.1G$ : 0.4 Vp-p to 1.0 Vp-p
Input Sensitivity (Eye Height)	NRZ: 19 mV @ 26.5625 Gbaud, 21 mV @ 53.125 Gbaud PAM4: 23 mV @ 26.5625 Gbaud, 36 mV @ 53.125 Gbaud
Clock Recovery (Option)	2.4 Gbaud to 32.1 Gbaud, 51 Gbaud to 58.2 Gbaud
Equalizer (Option)	Low-frequency Equalizer ( $\leq 1$ GHz, 2 dB typ.) + DFE (1.4 dB typ.)
PAM4 Patterns	SSPRQ, PRBS13Q, PRBS31Q, etc.
PAM4 Counter	MSB, LSB, Symbol 0 to 3 (Option)
Input Connector	V (f)

## Signal Quality Analyzer-R MP1900A Specifications

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### 32G baud NRZ/PAM4 Re-Driver MU196060A

Target Applications	PCIe 4.0: 16.0 Gbit/s, NRZ PCIe 5.0: 32.0 Gbit/s, NRZ PCIe 6.0: 32.0 Gbaud, PAM4 IEEE802.3bs 400GAUI-8 C2M: 26.5625 Gbaud, PAM4
Supported Plug-in Modules	MU196040B PAM4 ED MU195040A 21G/32G bit/s SI ED
Input Amplitude	<b>PAM4:</b> 0.40 to 0.80 Vp-p / Differential BER < 1E-8, 1E-12 (typ.), MCP, SSC 5300 ppm Down spread <b>NRZ:</b> 0.18 to 0.80 Vp-p / Differential BER < 1E-12, MCP, SSC 5300 ppm Down spread
Input/Output Connector	V (f)
LOSS Compensation	<b>PAM4:</b> 14 dB at 16.0 GHz, BER < 1E-6, 1E-9 (typ.), MCP, SSC 5300 ppm Down spread <b>NRZ:</b> 30 dB at 16.0 GHz, BER < 1E-12, MCP, SSC 5300 ppm Down spread
Clock Recovery (option)	With SSC support, PCIe Gen 4.0, 5.0, 6.0

# Signal Quality Analyzer-R MP1900A Ordering Information

When ordering, determine the configuration by referencing the selection guide (MP1900A-E-Z-1) and specify the type, model, name, and quantity. The names listed in the chart below are Order Names. The actual name of the item may differ from the Order Name.

## MP1900A

Model/Order No.	Name
MP1900A	<b>Main Frame*1</b> Signal Quality Analyzer-R
	<b>Standard Accessories</b>
G0342A	ESD DISCHARGER: 1
J1211	POWER CORD. 3M: 1
J1627A	GND connection cable: 1
P0031A	USB Memory: 1
Z0306A	Wrist Strap: 1
-	RJ45 Cap (Cap for Ethernet Port): 1
MX190000A	Signal Quality Analyzer-R Control Software*2
MX183000A	High-Speed Serial Data Test Software*3, *4
	<b>Retrofit Option</b>
MP1900A-110	Windows10 Upgrade Retrofit*5
	<b>Maintenance Service</b>
MP1900A-ES310	Three Years Extended Warranty Service
MP1900A-ES510	Five Years Extended Warranty Service

\*1: The Windows 10 OS will be installed in all orders from July 1, 2020.

\*2: Standard software pre-installed in Signal Quality Analyzer-R MP1900A

\*3: Trial software pre-installed in Signal Quality Analyzer-R MP1900A for extending functions with 30-day free trial period following first launch. When requiring the official version after the 30-day trial period, obtain the official license by purchasing the separate MX183000A-PLxx software license. Refer to the software license.

\*4: The PAM4 Control function is bundled with the MX183000A as a standard function and can be used without a license.

\*5: MP1900A main units running Windows Embedded Standard 7 are retrofitted to Windows 10 using a hardware upgrade. Anritsu destroys the unnecessary, post-upgrade Windows Embedded Standard 7 parts. For details, contact our sales representative.

## MU181000B

Model/Order No.	Name
MU181000B	<b>Module</b> 12.5 GHz 4port Synthesizer
	<b>Standard Accessories</b>
J1624A	Coaxial Cable 0.3 m (SMA): 4 pcs
	<b>Option</b>
MU181000B-002	SSC Extension
	<b>Retrofit Option</b>
MU181000B-102	SSC Extension Retrofit
	<b>Maintenance Service</b>
MU181000B-ES310	Three Years Extended Warranty Service
MU181000B-ES510	Five Years Extended Warranty Service

## MU181500B

Model/Order No.	Name
MU181500B	<b>Module</b> Jitter Modulation Source
	<b>Standard Accessories</b>
J1624A	Coaxial Cable 0.3 m (SMA): 1 pc
J1508A	BNC-SMA Connector Cable (30 cm): 2 pcs
J1137	Terminator: 6 pcs
J1341A	Open: 2 pcs
Z0897A	MP1800A Manual CD: 1 pc
Z0918A	MX180000A Software CD: 1 pc
	<b>Maintenance Service</b>
MU181500B-ES310	Three Years Extended Warranty Service
MU181500B-ES510	Five Years Extended Warranty Service

## MU195050A

Model/Order No.	Name
MU195050A	<b>Module</b> Noise Generator
	<b>Standard Accessories</b>
J1632A	Terminator (SMA): 4
J1359A	Coaxial Adapter (K-P, K-J, SMA): 4
J1717A	COAXIAL ADAPTOR (SMA-P, SMA-J): 2
J1341A	Open: 6
J1746A	Skew Match Pair Semrigid Cable (K connector, Data Input1): 1 set
J1747A	Skew Match Pair Semrigid Cable (K connector, Data Input2): 1 set
J1792A	Skew Match Pair Semrigid Cable (V-K connector, MU196020A PPG Output to MU195050A Noise Data Input1): 1 set
	<b>Option</b>
MU195050A-001	White Noise
	<b>Retrofit Option</b>
MU195050A-101	White Noise Retrofit
	<b>Maintenance Service</b>
MU195050A-ES310	Three Years Extended Warranty Service
MU195050A-ES510	Five Years Extended Warranty Service

## MU196060A\*13

Model/Order No.	Name
MU196060A	<b>Module</b> 32G baud NRZ/PAM4 Re-Driver
	<b>Standard Accessories</b>
J1916A	OPEN (V): 4 pcs
J1341A	OPEN (SMA): 1 pc
J1898A	Coaxial Cable Set for MU196060A: 1 set
	[ J1917A Coaxial Semi-rigid Cable: 1
	J1932A Coaxial Skew Matched Cable Pair (0.8 m, V Connector): 1 ]
	<b>Option</b>
MU196060A-001	Clock Recovery for SSC
	<b>Retrofit Option</b>
MU196060A-301	Clock Recovery for SSC Retrofit
	<b>Maintenance Service</b>
MU196060A-ES310	Three Years Extended Warranty Service
MU196060A-ES510	Five Years Extended Warranty Service

# Signal Quality Analyzer-R MP1900A Ordering Information

When ordering, determine the configuration by referencing the selection guide (MP1900A-E-Z-1) and specify the type, model, name, and quantity.

## MU195020A

Model/Order No.	Name
MU195020A	<b>Module</b> 21G/32G bit/s SI PPG
<b>Standard Accessories</b>	
J1632A	Terminator (SMA): 5
J1341A	Open: 2
J1359A	Coaxial Adapter (K-P, K-J, SMA): 1
J1717A	COAXIAL ADAPTOR (SMA-P, SMA-J): 6
<b>Option</b>	
MU195020A-001	32G bit/s Extension
MU195020A-010	1ch Data Output
MU195020A-020	2ch Data Output
MU195020A-011	1ch 10Tap Emphasis
MU195020A-021	2ch 10Tap Emphasis
MU195020A-030	1ch Data Delay
MU195020A-031	2ch Data Delay
MU195020A-040	1ch Variable ISI
MU195020A-041	2ch Variable ISI
MU195020A-050	Sequence Editor Function*6
MU195020A-051	Sequence Editor Function PCIe 5 Extension*6
<b>Retrofit Options</b>	
MU195020A-101	32G bit/s Extension Retrofit
MU195020A-111	1ch 10Tap Emphasis Retrofit
MU195020A-121	2ch 10Tap Emphasis Retrofit
MU195020A-130	1ch Data Delay Retrofit
MU195020A-131	2ch Data Delay Retrofit
MU195020A-140	1ch Variable ISI Retrofit
MU195020A-141	2ch Variable ISI Retrofit
MU195020A-340	1ch Variable ISI Retrofit
MU195020A-341	2ch Variable ISI Retrofit
MU195020A-350	Sequence Editor Function Retrofit
MU195020A-351	Sequence Editor Function PCIe 5 Extension Retrofit
<b>Opt-x10 Accessories</b>	
J1632A	Terminator (SMA): 2
J1359A	Coaxial Adapter (K-P, K-J, SMA): 2
<b>Opt-x20 Accessories</b>	
J1632A	Terminator (SMA): 4
J1359A	Coaxial Adapter (K-P, K-J, SMA): 4
<b>Maintenance Service</b>	
MU195020A-ES310	Three Years Extended Warranty Service
MU195020A-ES510	Five Years Extended Warranty Service

\*6: Option 050 supports PCIe Gen 1 to Gen 4, and USB 3.2 × 1. Option 051 supports PCIe Gen5. Option 050 is required when adding Option 051.

## MU196020A\*13

Model/Order No.	Name
MU196020A	<b>Module</b> PAM4 PPG
<b>Standard Accessories</b>	
J1632A	TERMINATOR: 4
J1889A	TERMINATOR (V): 2
J1341A	OPEN: 2
J1359A	COAXIAL ADAPTOR (K-P.K-J,SMA): 1
J1717A	COAXIAL ADAPTOR(SMA-P.SMA-J): 5
<b>Option</b>	
MU196020A-001	32G baud*
MU196020A-002	58G baud*
MU196020A-003	64G baud*
MU196020A-011	4Tap Emphasis
MU196020A-030	Data Delay
MU196020A-040	Adjustable ISI
MU196020A-042	FEC Pattern Generation
MU196020A-043	FEC Error Insertion for PCIe6
MU196020A-045	USB4 Gen4 Pattern Generation
MU196020A-050	Inter-Module Synchronization
MU196020A-051	Sequence Editor Function
MU196020A-052	Sequence Editor Function for Multi-channel
MU196020A-060	PCIe6 LEQ
<b>Retrofit Options</b>	
MU196020A-112	32G to 58G baud Extension Retrofit
MU196020A-113	32G to 64G baud Retrofit
MU196020A-123	58G to 64G baud Retrofit
MU196020A-111	4Tap Emphasis Retrofit
MU196020A-130	Data Delay Retrofit
MU196020A-140	Adjustable ISI Retrofit
MU196020A-142	FEC Pattern Generation Retrofit
MU196020A-145	USB4 Gen4 Pattern Generation Retrofit
MU196020A-150	Inter-Module Synchronization Retrofit
MU196020A-160	PCIe6 LEQ Retrofit
MU196020A-340	Adjustable ISI Retrofit
MU196020A-342	FEC Pattern Generation Retrofit
MU196020A-343	FEC Error Insertion for PCIe6 Retrofit
MU196020A-345	USB4 Gen4 Pattern Generation Retrofit
MU196020A-351	Sequence Editor Function Retrofit
MU196020A-352	Sequence Editor Function for Multi-channel Retrofit
MU196020A-360	PCIe6 LEQ Retrofit*7
<b>Maintenance Service</b>	
MU196020A-ES310	Three Years Extended Warranty Service
MU196020A-ES510	Five Years Extended Warranty Service

\*7: Order when MU196020A serial number is 6272477551 or later

\*: Select any one

# Signal Quality Analyzer-R MP1900A Ordering Information

When ordering, determine the configuration by referencing the selection guide (MP1900A-E-Z-1) and specify the type, model, name, and quantity.

## MU195040A

Model/Order No.	Name
MU195040A	<b>Module</b> 21G/32G bit/s SI ED
<b>Standard Accessories</b>	
J1632A	Terminator (SMA): 2
J1341A	Open: 1
J1717A	COAXIAL ADAPTOR (SMA-P, SMA-J): 4
<b>Option</b>	
MU195040A-001	32G bit/s Extension
MU195040A-010	1ch ED
MU195040A-020	2ch ED
MU195040A-011	1ch CTLE
MU195040A-021	2ch CTLE
MU195040A-022	Clock Recovery
<b>Retrofit Options</b>	
MU195040A-101	32G bit/s Extension Retrofit
MU195040A-111	1ch CTLE Retrofit
MU195040A-121	2ch CTLE Retrofit
MU195040A-122	Clock Recovery Retrofit
<b>Opt-x10 Accessories</b>	
J1341A	Open: 3
J1359A	Coaxial Adapter (K-P, K-J, SMA): 2
J1887A	Fixed Attenuator (6 dB, K Connector): 2
<b>Opt-x20 Accessories</b>	
J1341A	Open: 5
J1359A	Coaxial Adapter (K-P, K-J, SMA): 4
J1887A	Fixed Attenuator (6 dB, K Connector): 4
<b>Maintenance Service</b>	
MU195040A-ES310	Three Years Extended Warranty Service
MU195040A-ES510	Five Years Extended Warranty Service

## MU196040B\*13

Model/Order No.	Name
MU196040B	<b>Module</b> PAM4 ED
<b>Standard Accessories</b>	
J1632A	TERMINATOR: 2
J1889A	TERMINATOR (V): 2
J1341A	OPEN: 2
J1359A	COAXIAL ADAPTOR (K-P.K-J,SMA): 1
J1717A	COAXIAL ADAPTOR (SMA-P.SMA-J): 3
J1888A	Fixed Attenuator 6 dB: 2
<b>Option</b>	
MU196040B-001	32G baud (2.4G to 32.1G)*
MU196040B-002	58G baud (NRZ: 2.4G to 64.2G, PAM4: 2.4G to 58.2G)*
MU196040B-011	Equalizer
MU196040B-021	29G baud Clock Recovery (2.4G to 29G)* <sup>8</sup>
MU196040B-022	32G baud Clock Recovery (2.4G to 32.1G)* <sup>8</sup>
MU196040B-023	58G baud Clock Recovery Extension (51G to 58.2G)* <sup>8</sup>
MU196040B-041	SER Measurement
MU196040B-042	FEC Analysis
MU196040B-043	FEC Analysis for PCIe6
MU196040B-051	PCIe Sequence Editor Pattern Analysis
<b>Retrofit Options</b>	
MU196040B-111	Equalizer Retrofit
MU196040B-112	32G to 58G baud Extension Retrofit
MU196040B-121	29G baud Clock Recovery Retrofit
MU196040B-122	32G baud Clock Recovery Retrofit
MU196040B-123	58G baud Clock Recovery Extension Retrofit
MU196040B-124	32G baud Clock Recovery Extension Retrofit
MU196040B-141	SER Measurement Retrofit
MU196040B-341	SER Measurement Retrofit
MU196040B-342	FEC Analysis Retrofit
MU196040B-343	FEC Analysis for PCIe6 Retrofit
MU196040B-351	PCIe Sequence Editor Pattern Analysis Retrofit
<b>Maintenance Service</b>	
MU196040B-ES310	Three Years Extended Warranty Service
MU196040B-ES510	Five Years Extended Warranty Service

\*8: Select at least one option; either Option 021 or 022 is required when adding Option 023.

\*: Select any one

## Signal Quality Analyzer-R MP1900A Ordering Information

When ordering, determine the configuration by referencing the selection guide (MP1900A-E-Z-1) and specify the type, model, name, and quantity.

### MU183020A

Model/Order No.	Name
MU183020A	<b>Module</b> 28G/32G bit/s PPG
<b>Standard Accessories</b>	
J1137	Terminator: 3 pcs
J1359A	Coaxial Adaptor (K-P, K-J, SMA): 1 pc
J1341A	Open: 1 pc
J0541E	6 dB Fixed Attenuator: 1 pc
Z0897A	MP1800A Manual CD: 1 pc
Z0918A	MX180000A Software CD: 1 pc
<b>Options</b>	
MU183020A-001	32G bit/s Extension
MU183020A-012	1ch 2 V Data Output
MU183020A-013	1ch 3.5 V Data Output
MU183020A-022	2ch 2 V Data Output
MU183020A-023	2ch 3.5 V Data Output
MU183020A-030	1ch Data Delay
MU183020A-031	2ch Data Delay
<b>Retrofit Options</b>	
MU183020A-101	32G bit/s Extension Retrofit
MU183020A-112	1ch 2 V Data Output Retrofit
MU183020A-113	1ch 3.5 V Data Output Retrofit
MU183020A-122	2ch 2 V Data Output Retrofit
MU183020A-123	2ch 3.5 V Data Output Retrofit
MU183020A-130	1ch Data Delay Retrofit
MU183020A-131	2ch Data Delay Retrofit
<b>Standard Accessories for MU183020A-x12, x13</b>	
J1137	Terminator: 2 pcs
J1359A	Coaxial Adaptor (K-P, K-J, SMA): 2 pcs
<b>Standard Accessories for MU183020A-x22, x23</b>	
J1137	Terminator: 4 pcs
J1359A	Coaxial Adaptor (K-P, K-J, SMA): 4 pcs
<b>Maintenance Service</b>	
MU183020A-ES310	Three Years Extended Warranty Service
MU183020A-ES510	Five Years Extended Warranty Service

### MU183040B

Model/Order No.	Name
MU183040B	<b>Module</b> 28G/32G bit/s High Sensitivity ED
<b>Standard Accessories</b>	
J1137	Terminator: 2 pcs
J1341A	Open: 1 pc
Z0897A	MP1800A Manual CD: 1 pc
Z0918A	MX180000A Software CD: 1 pc
<b>Options</b>	
MU183040B-001	32 Gbit/s Extension
MU183040B-010	1ch ED
MU183040B-020	2ch ED
MU183040B-022	2.4G to 28.1G bit/s Clock Recovery
MU183040B-023	25.5G to 32.1G bit/s Clock Recovery
<b>Retrofit Options</b>	
MU183040B-101	32 Gbit/s Extension Retrofit
MU183040B-110	1ch ED Retrofit
MU183040B-120	2ch ED Retrofit
MU183040B-122	2.4G to 28.1G bit/s Clock Recover Retrofit
MU183040B-123	25.5G to 32.1G bit/s Clock Recovery Retrofit
<b>Standard Accessories for MU183040B-x10</b>	
J1341A	Open: 2 pcs
J1359A	Coaxial Adaptor (K-P, K-J, SMA): 2 pcs
41KC-6	Precision Fixed Attenuator 6 dB: 2 pcs
<b>Standard Accessories for MU183040B-x20</b>	
J1341A	Open: 4 pcs
J1359A	Coaxial Adaptor (K-P, K-J, SMA): 4 pcs
41KC-6	Precision Fixed Attenuator 6 dB: 4 pcs
<b>Maintenance Service</b>	
MU183040B-ES310	Three Years Extended Warranty Service
MU183040B-ES510	Five Years Extended Warranty Service

# Signal Quality Analyzer-R MP1900A Ordering Information

When ordering, determine the configuration by referencing the selection guide (MP1900A-E-Z-1) and specify the type, model, name, and quantity.

## Software License

Model/Order No.	Name
MX183000A	High-Speed Serial Data Test Software
MX183000A-PL001	Jitter Tolerance Test
MX183000A-PL011	PCIe Link Sequence
MX183000A-PL021	PCIe Link Training <sup>*9</sup>
MX183000A-PL022	USB Link Training <sup>*10</sup>
MX183000A-PL023	USB 3.2 × 2 Link Training <sup>*10</sup>
MX183000A-PL025	PCIe 5 Link Training <sup>*9</sup>
MX183000A-PL026	PCIe 6 Link Training <sup>*9</sup>
MX183000A-PL031	DUT Error Counts Import

\*9: PL021 supports PCIe Gen1 to Gen4.

PL025 supports PCIe Gen5.

PL026 supports PCIe Gen6.

Requires PL021 to add PL025.

Requires PL021 and PL025 to add PL026.

\*10: PL022 supports USB 3.2 × 1. PL023 supports USB 3.2 × 2. PL022 is required to add PL023.

## On Using VISA<sup>\*11</sup>

The National Instruments™ (NI hereafter) NI-VISA<sup>\*12</sup> software must be installed to use the MX183000A (this product hereafter). We recommend using NI-VISA saved on the product USB memory stick. Customers may only use NI-VISA saved on the product memory stick. NI-VISA on the memory stick may not be used for other applications with other products. When uninstalling this product from the controller PC, etc., also uninstall NI-VISA from the USB memory.

\*11: Abbreviation for Virtual Instrument Software Architecture. This is I/O software for remote control of measuring instruments via GPIB, Ethernet and USB interfaces.

\*12: NI-VISA was developed by National Instruments for VXI Plug&Play Alliance standards compliant I/O interfaces. National Instruments™, NI™, and NI-VISA™ are registered trademarks of National Instruments Corporation.

## Optional Accessories

Model/Order No.	Name
J1900A	Passive Low Frequency Equalizer
J1632A	Terminator (SMA)
J1889A	TERMINATOR (V)
J1678A	ESD Protection Adapter-K
J1679A	ESD Protection Adapter-V
J1359A	Coaxial Adapter (K-P, K-J, SMA)
34VFK50A	Fixed Adapter (V-F, K-M) <sup>*13</sup>
34VFK50A	Fixed Adapter (V-M, K-F) <sup>*13</sup>
41KC-3	Fixed Attenuator 3 dB
41KC-6	Fixed Attenuator 6 dB
41KC-10	Fixed Attenuator 10 dB
41KC-20	Fixed Attenuator 20 dB
41VA-3	Fixed Attenuator 3 dB
41VA-6	Fixed Attenuator 6 dB
41VA-10	Fixed Attenuator 10 dB
41VA-20	Fixed Attenuator 20 dB
J1887A	Fixed Attenuator (6 dB, K Connector)
J1888A	Fixed Attenuator (6 dB, V Connector)
J1758A	ISI Board
J1800A	ISI Board V
K261	DC Block
K240C	Precision Power Divider
V240C	Fixed Power divider
J1510A	Pick OFF Tee (K)
J1793A	Pick OFF Tee (V)
K241C	Power Splitter
J1748A	Power Splitter (1.5 GHz to 18 GHz, SMA, using MU195020A × 4 to MU181500B connection)
J1624A	COAXIAL CABLE 0.3 m (SMA connector)
J1342A	COAXIAL CABLE 0.8 m (APC3.5 connector)
J1439A	Coaxial cable (0.8 m, K connector)
J1625A	Coaxial Cable 1 m (SMA connector)
J1449A	Measurement kit (J1324A × 2, J1439A × 2, J1625A × 1)
J1550A	Coaxial skew match cable (0.8 m, APC3.5 connector)
J1551A	Coaxial skew match cable (0.8 m, K connector)
J1728A	Electrical Length Specified Coaxial Cable (0.4 m, K connector) <sup>*13</sup>
J1741A	Electrical Length Specified Coaxial Cable (0.8 m, K Connector) <sup>*13</sup>
J1789A	Electrical Length Specified Coaxial Cable (0.4 m, V connector) <sup>*13</sup>
J1790A	Electrical Length Specified Coaxial Cable (0.8 m, V connector) <sup>*13</sup>
J1792A	Skew match pair semirigid cable (V-K connector, MU196020A PPG Output to MU195050A Noise Data Input1)
J1898A	Coaxial Cable Set for MU196060A
J1917A	Coaxial Semi-rigid Cable
J1932A	Coaxial Skew Matched Cable Pair (0.8 m, V Connector)
J1761A	PCIe Reference Clock Cable Kit
Z2025A	PCIe CBB Controller
Z2029A	PCIe Reference Clock Buffer
AH54192A	56Gbaud Differential Linear Amplifier
W3911AE	MP1900A Operation Manual
W3913AE	MX190000A Operation Manual
W3813AE	MX183000A Operation Manual
W3915AE	MU195020/40/50A Operation Manual
W3976AE	MU196020/40A OPERATION MANUAL
B0576A	Blank Panel
B0736A	Front Cover (For MP1900A)
B0737A	Carrying Case (For MP1900A, with B0736A)
B0738A	Rack Mount Kit (For MP1900A)
Z1746A	Stylus
Z0541A	USB Mouse
J0008	GPIB CABLE, 2.0 m
Z0917A	Shielded LAN Cable, 5 m
Z1953A	Gigabit Ethernet Switch (5 Port)
Z0306A	Wrist Strap
Z1964A	Torque Wrench (Right Angle)

# Signal Quality Analyzer-R MP1900A Ordering Information

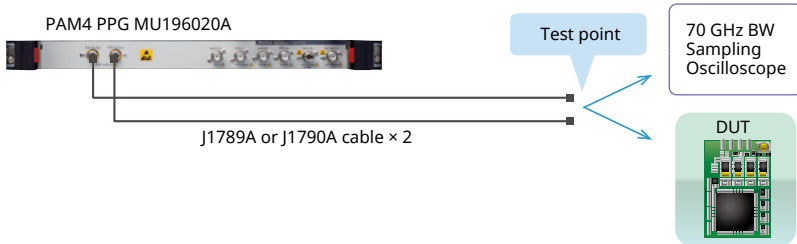
When ordering, determine the configuration by referencing the selection guide (MP1900A-E-Z-1) and specify the type, model, name, and quantity.

## J1815A MP1900A PCIe Measurement Component Set

The following table lists the component set required by the PCIe Gen3/4/5 Tx/Rx LEQ test.

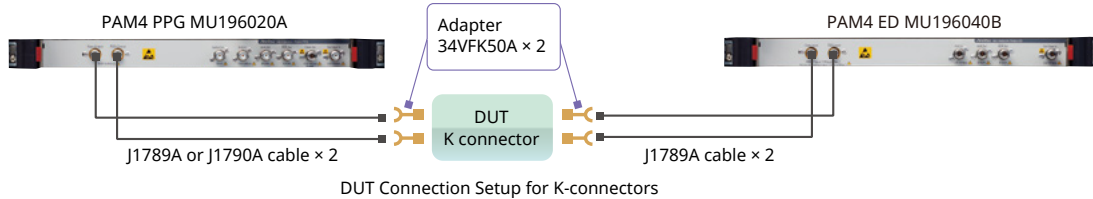
Item	Description	Qty.	Remarks		
Optional Accessories	MP1900A PCIe Measurement Component Set	1	J1815A		
			Accessories	Qty.	Comment
			Coax skew match cable, 0.8 m K connector	4	Junflon J12J103220-00-1
			AE-TMC-10205	2	Coax cable, 1 m, SMA connector
			PICK OFF TEE	2	Anritsu 3-68231
			SMPF-SMAJ-TFLEX-10CM-5PS	2	SMP to SMA adapter cable
			BNC-SMA cable	2	
			K261	2	DC Block
K241C	2	Power Splitter			

\*13: We recommend using either the J1789A or J1790A as the coaxial cable for the MU196020A data output. Recommend using coaxial cable J1789A for MU196040B Data IN. The MU196020A data output specifications are defined based on the performance observed using a 70-GHz bandwidth oscilloscope connected as shown below.



### Solution except above

The MU196020A Data OUT and MU196040B Data IN connectors, and the J1789A/J1790A cables all use V-connectors. Consequently, for K-connectors, use 34VFK50 adapters as shown in the following figure.

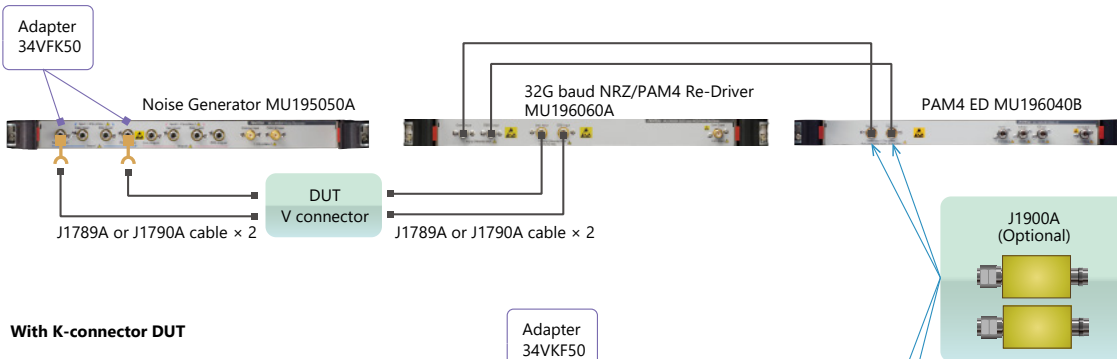


### PCIe and Ethernet (26.5625 Gbaud) Solution

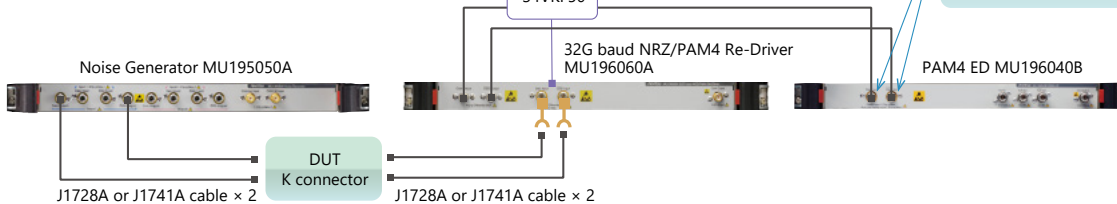
The MU195050A Data output uses a K-connector. The MU196060A Data input uses a V-connector. Use the 34VFK50 or 34VKF50 adapter that matches the DUT type.

Also, when using the J1900A, connect it to the Data Input of the MU196040A as shown in the diagram below. An additional pair (2 pieces) of 34VFK50 adapters is required when using the MU196060A and MU195040A in combination. The J1900A is not required when using the MU195040A.

#### With V-connector DUT



#### With K-connector DUT







Specifications are subject to change without notice.

• **United States**

**Anritsu Americas Sales Company**

490 Jarvis Drive, Morgan Hill, CA 95037-2809, U.S.A.  
Phone: +1-800-Anritsu (1-800-267-4878)

• **Canada**

**Anritsu Electronics Ltd.**

**Americas Sales and Support**

490 Jarvis Drive, Morgan Hill, CA 95037-2809, U.S.A.  
Phone: +1-800-Anritsu (1-800-267-4878)

• **Brazil**

**Anritsu Eletrônica Ltda.**

Praça Amadeu Amaral, 27 - 1 Andar  
01327-010 - Bela Vista - Sao Paulo - SP, Brazil  
Phone: +55-11-3283-2511  
Fax: +55-11-3288-6940

• **Mexico**

**Anritsu Company, S.A. de C.V.**

Bldv Miguel de Cervantes Saavedra #169 Piso 1, Col. Granada  
Mexico, Ciudad de Mexico, 11520, MEXICO  
Phone: +52-55-4169-7104

• **United Kingdom**

**Anritsu EMEA Limited**

900 Capability Green, Luton, Bedfordshire, LU1 3LU, U.K.  
Phone: +44-1582-433200  
Fax: +44-1582-731303

• **France**

**Anritsu SA**

12 avenue du Québec, Immeuble Goyave,  
91140 VILLEBON SUR YVETTE, France  
Phone: +33-1-60-92-15-50

• **Germany**

**Anritsu GmbH**

Nemetschek Haus, Konrad-Zuse-Platz 1,  
81829 München, Germany  
Phone: +49-89-442308-0  
Fax: +49-89-442308-55

• **Italy**

**Anritsu S.R.L.**

Spaces Eur Arte, Viale dell'Arte 25, 00144 Roma, Italy  
Phone: +39-6-509-9711

• **Sweden**

**Anritsu AB**

Kistagången 20 B, 2 tr, 164 40 Kista, Sweden  
Phone: +46-8-534-707-00

• **Finland**

**Anritsu AB**

Technopolis Aviapolis, Teknobulevardi 3-5 (D208.5),  
FI-01530 Vantaa, Finland  
Phone: +358-20-741-8100

• **Denmark**

**Anritsu A/S**

c/o Regus Winghouse, Ørestads Boulevard 73, 4th floor,  
2300 Copenhagen S, Denmark  
Phone: +45-7211-2200

• **Spain**

**Anritsu EMEA GmbH**

**Representation Office in Spain**

Calle Manzanares 4, Primera planta, 28005 Madrid, Spain  
Phone: +34-91-572-6761

• **Austria**

**Anritsu EMEA GmbH**

Am Belvedere 10, A-1100 Vienna, Austria  
Phone: +43-(0)1-717-28-710

• **United Arab Emirates**

**Anritsu A/S**

Office No. 164, Building 17, Dubai Internet City  
P. O. Box – 501901, Dubai, United Arab Emirates  
Phone: +971-4-3758479

• **India**

**ANRITSU INDIA PRIVATE LIMITED**

6th Floor, Indiqube ETA, No.38/4, Adjacent to EMC2,  
Doddanekundi, Outer Ring Road, Bengaluru – 560048, India  
Phone: +91-80-6728-1300  
Fax: +91-80-6728-1301

• **Singapore**

**ANRITSU PTE LTD**

1 Jalan Kilang Timor, #07-04/06 Pacific Tech Centre  
Singapore 159303  
Phone: +65-6282-2400  
Fax: +65-6282-2533

• **Vietnam**

**ANRITSU COMPANY LIMITED**

16th Floor, Peakview Tower, 36 Hoang Cau Street, O Cho Dua Ward,  
Hanoi, Vietnam  
Phone: +84-24-3201-2730  
Fax: +84-24-3201-2740

• **P.R. China (Shanghai)**

**Anritsu (China) Co., Ltd.**

Room 2301-2303, Tower A, New Caohejing International Business  
Center No. 391 Gui Ping Road, Shanghai, 200233, P.R. China  
Phone: +86-21-6237-0898  
Fax: +86-21-6237-0899

• **P.R. China (Hong Kong)**

**ANRITSU COMPANY LIMITED**

Unit 1302, 13<sup>th</sup> Floor, New East Ocean Center,  
No.9 Science Museum Road, TsimShaTsui East,  
Kowloon, Hong Kong  
Phone: +852-2301-4980  
Fax: +852-2301-3545

• **Japan**

**Anritsu Corporation**

8-5, Tamura-cho, Atsugi-shi, Kanagawa, 243-0016 Japan  
Phone: +81-46-296-6509  
Fax: +81-46-225-8352

• **Korea**

**Anritsu Corporation Limited**

8F, A TOWER, 20, Gwacheondaero 7-gil, Gwacheon-si,  
Gyeonggi-do, 13840, Republic of Korea  
Phone: +82-2-6259-7300  
Fax: +82-2-6259-7301

• **Australia**

**Anritsu Pty Ltd**

Unit 20, 21-35 Ricketts Road, Mount Waverley, Victoria 3149, Australia  
Phone: +61-3-9558-8177  
Fax: +61-3-9558-8255

• **Taiwan**

**ANRITSU COMPANY, INC.**

7F, No. 316, Sec. 1, NeiHu Rd., Taipei 114, Taiwan  
Phone: +886-2-8751-1816  
Fax: +886-2-8751-1817