

Summit™ Z516

PCI Express® 5.0 and Compute Express Link™ Protocol Exerciser



Product Capabilities

- Supports PCI Express 5.0 including:
 - Data rates of 2.5, 5.0, 8.0, 16.0 and 32.0 GT/s
 - Link widths of x1 through x16
- Error injection
- Provides traffic generation and host/device emulation
- Supports NVMe/NVMe-MI
- Emulate root complexes or device endpoints
- Exercise LTSSM state transitions
- Generate controlled error conditions to test error recovery routines
- Supports Exercising SMBus, MCTP
- Supports Exercising Sideband Signals
- Can be used in Common Clock and SRIS environments
- Supports Alternate Protocol
- PCIe IDE/DOE Support

CXL Exerciser

- Supports all three CXL device types; CXL.io, CXL.mem, and CXL.cache
- Generates ALMP requests
- Emulates CXL Hosts and Devices
- Supports normal (32.0 GT/s at x16) and degraded modes

Product Development Support for PCI Express 5.0 and CXL™!

The Summit Z516 exerciser is designed for developers who need a protocol test system supporting the PCI Express 5.0 and CXL specifications. Supporting traffic generation at data rates to 32.0 GT/s with link widths up to 16 lanes, the Summit Z516 is Teledyne LeCroy's latest PCI Express (PCIe®) protocol exerciser, leveraging years of experience in providing advanced protocol test and compliance tools to the PCI Express community.

The Summit Z516 supports full traffic generation and device/host emulation, and provides the industry a platform for development of standardized compliance test suites.

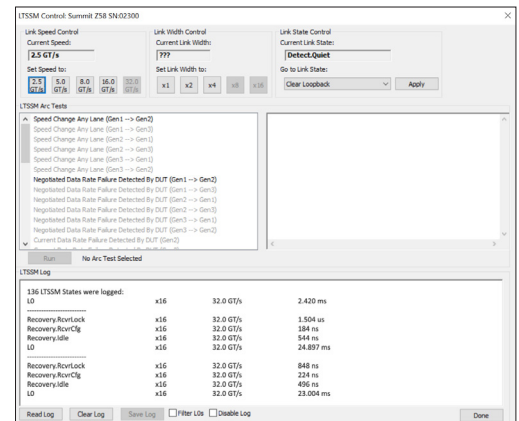
In addition, the system provides error injection functions to enable developers to test error recovery routines important to reliable interoperability of PCI Express 5.0 and CXL products.

rich programmable environment, scripting can be employed for full interoperability testing to improve the reliability of systems.

The Summit Z516 can emulate either PCIe and CXL root complexes or device endpoints, allowing new designs to be tested against known standards.

Typical Applications

The Summit Z516 is a critical test and verification tool to assist engineers in development, debug and validation of their PCIe and CXL designs (including early stage power-on testing). Because of its



A Wealth of PCI Express Features

Intuitive software controls blend sophisticated traffic generation when used with an external Summit series analyzer with ease-of-use, allowing test suites to be rapidly customized to meet specific test requirements. One feature that helps troubleshoot PCIe-based links is the ability to fully exercise the Link Training & Status State Machine (LTSSM) transitions. Powerful scripting language also allows for the creation of Transaction Layer Packets (TLPs) and Data Link Layer Packets (DLLPs) at PCIe 5.0 data rates of 32.0 GT/s. Flow Control and ACK/NAK's policies and structures can be defined and generated under user control.

Features addressing LTSSM structures include providing bus traffic to emulate all the states of the LTSSM from the Detect state, to the L0 state and maintaining the L0 state between the host and device. The exerciser also supports lane reversal and can control all polarity and scrambling configurations. An important feature to note is that traffic emulation supports dynamic equalization in addition to skipping the EQ phases entirely. The exerciser also has the capability to perform error injection for training sequences, as well as Data Link and Transaction Layer traffic, both at the packet level and on a per lane basis.

Packet fields not explicitly specified by the user are generated automatically (such as packet numbering and CRCs). The configuration space can be emulated for any device including endpoints, bridges and switches. Support for all PCIe 5.0 data rates allows the Summit Z516 to produce test cases that test the device's ability to auto-negotiate data rates with other devices.

In addition, the ability of the Summit Z516 to produce a wide variety of programmed traffic allows the user to introduce controlled error conditions. As an example, a trace file captured by the external Summit series PCIe protocol analyzer can be exported and used as the basis for a test script, with selected programmed errors introduced at critical stages to test the device's ability to recognize and recover from error conditions. This allows for detailed testing of simple error recovery and complex multiple error conditions, creating more resilient products that perform well even under less than ideal conditions.



Packet	R←	32.0	TLP	Mem	MWr(32)	Length	RequesterID	Tag	Address	1st BE	Last BE	Data	LCRC	Time Delta	Time Stamp	
1050		x16	3222		010:00000	32	001:00:0	0	DA000000	1111	1111	32 dwords	0x0F39C4DF	4.000 ns	0000 . 000 028 177 000 s	
Packet	R→	32.0	DLLP	ACK	AckNak_Seq_Num	CRC 16	Idle	Time Stamp								
1051		x16			3209	0x2517	30.500 ns	0000 . 000 028 181 000 s								
Packet	R→	32.0	DLLP	UpdateFC-P	HdrScale	HdrFC	DataScale	DataFC	CRC 16	Time Delta	Time Stamp					
1052		x16			1	218	1	3960	0xB94A	1.000 ns	0000 . 000 028 213 500 s					
Packet	R←	32.0	TLP	Mem	MWr(32)	Length	RequesterID	Tag	Address	1st BE	Last BE	Data	LCRC	Idle	Time Stamp	
1053		x16	3223		010:00000	32	001:00:0	0	DA000000	1111	1111	32 dwords	0x7B8BA620	2.180 ns	0000 . 000 028 214 500 s	
Packet	R←	32.0	EDS	EDS Symbols	Idle	Time Stamp										
1054		x16		1F 80 90 00	0.000 ns	0000 . 000 028 254 250 s										
Packet	R←	32.0	SKIP	SKIP Symbols	END	P	FR	SR	CRC	MP	UM	MT	RN	Payload	Idle	Time Stamp
1055		x16		99 99 99 99 99 ...	78	1	1	1	25	0	0	7	0	156	0.000 ns	0000 . 000 028 255 250 s

Full CXL Traffic Generation and Error Insertion Capabilities

Compute Express Link (CXL) is a new high-speed CPU-to-Device and CPU-to-Memory interconnect designed to accelerate next-generation data center performance. CXL is based on the PCI Express 5.0 Physical layer with speeds up to 32.0 GT/s. The exerciser scripting language also allows for the creation of CXL Transaction Layer Packets (CXL.io TLPs) and Data Link Layer Packets (CXL.io DLLPs) in addition to CXL.mem and CXL.cache requests at PCIe 5.0 data rates of 32.0 GT/s. Flow Control and acknowledge policies and Flit structures for each of the CXL protocols: CXL.io, CXL.mem, CXL.cache can be defined and generated under user control.

Packet	2.5	TS1_MOD	COM	Link	Lane	N	FTS	Training Control	Data Rate	TS1 Symbols	Usage	Alt Prot Status	Alt Prot ID	Cmn Clk	Vendor ID	PCIe	CXL.IO	CXL.CACHE
7	R→	x4	K28.5	247	0	42	0 0 0 0 0 1 1	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s, 32.0 GT/s	D10.2 ...	AltProtNegotiation	0	0	0	0x	0	1	1	
CXL.MEM			Retimer1	SH Bypass	Retimer2	Parity	Idle	Time Stamp										
1			1	1	0	0xE0	10.000 ms	0000 . 080 000 700 000 s										

Modified TS1 displaying alternate protocol information

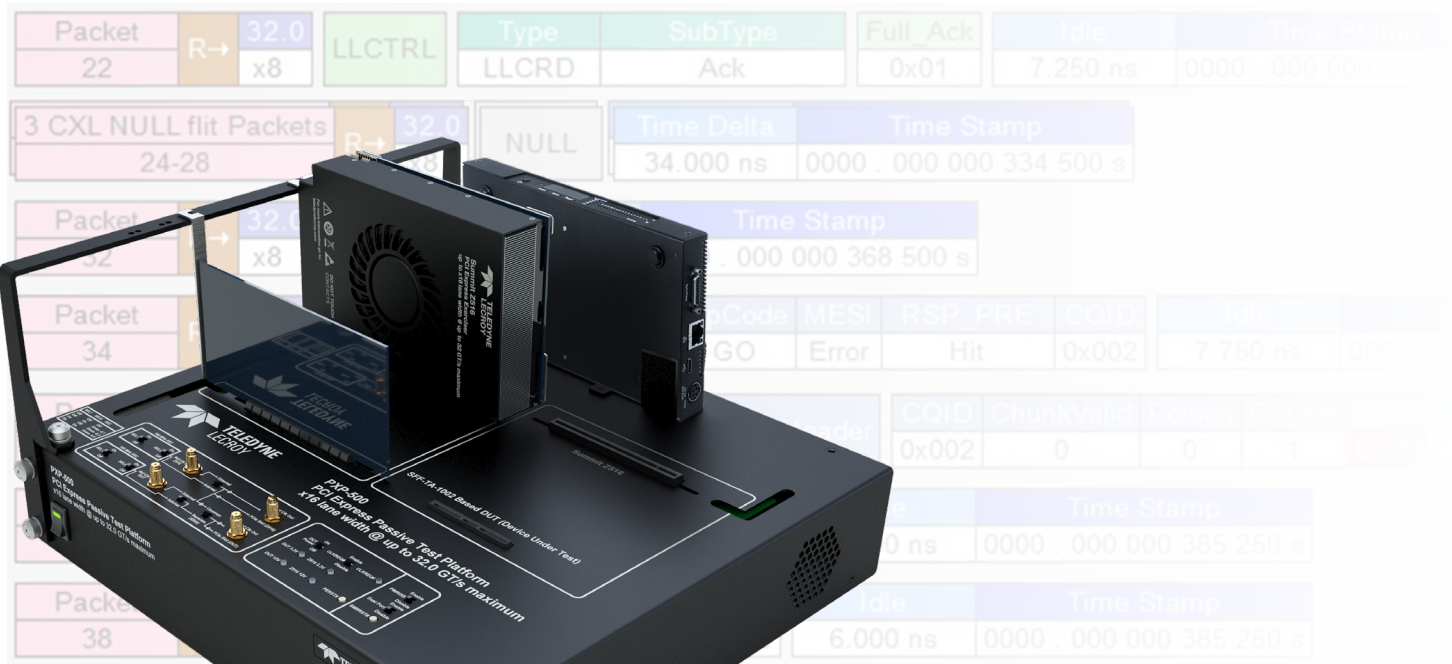
The Summit Z516 can also generate CXL.io, CXL.cache, and CXL.mem packets that can be dynamically multiplexed on the link. It can provide traffic and error generation for systems through all layers from the FlexBus Physical layer and Flits all the way up to the Link and Transaction Layers.

Usage	Alt Prot Status	Alt Prot ID	Cmn Clk	Vendor ID	PCIe	CXL.IO	CXL.CACHE	CXL.MEM	Retimer1	SH Bypass	Retimer2	Parity
AltProtNegotiation	0	0	0	0x	0	1	1	1	1	1	0	0xE0

Alternate Protocol displaying CXL.io, CXL.cache, and CXL.mem fields in trace

Packet	32.0	ALMP	Type	VLSM State	Target	Idle	Time Stamp
2	R→	x8	Request	ACTIVE	CXL.io	10.000 ms	0000 . 030 000 200 000 s

The ARB/Mux Link Management Packet (ALMP) can be generated by using the Exerciser



PXP-500 Test Platform

The protocol exerciser uses a test platform with both CEM and SFF-TA-1002 connectors for connectivity to the DUT. This CXL protocol exerciser solution will provide a useful tool for early testing and when combined with the PCIe Protocol Analyzer it will help shorten development and testing time. The exerciser can be used with or without the PXP-500 depending on application, and can also plug into a standard CEM slot when being used as a device.

Specifications

Host Machine Minimum Requirements	64-bit (x64) versions of Windows® 11, Windows 10, Windows Server 2016, and Windows Server 2019. o The latest Service Pack available for the Windows OS in use is required. 4 GB of RAM; storage with at least 2 GB of free space for the installation of the software and additional space for recorded data; display with resolution of at least 1024x768 with at least 16-bit color depth; USB 2.0/3.0/3.1 port and/ or 100/1000 Mbps Ethernet network interface. For optimal performance, please refer to our recommended configuration in the product documentation.
Data Rates Supported	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s and 32.0 GT/s (PCI Express 5.0)
Ports	Summit Z516 x16 Plug-In Card: Connector cable to Summit Z516 controller Summit Z516 Controller: Connector to Interposer, USB Type-C, 1000BASE-T Ethernet, Sync/Data, DC Power (from supplied adapter)
Display Panel	Eight character alphanumeric display
LEDs	Power LED, Status LED, Trigger LED, Four Data Rate LEDs (2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s, 32.0 GT/s) Activity LEDs (2 per lane—Tx/Rx—for 16 lanes), Training LED
Dimensions and Weight	Summit Z516 Plug-In Card: 39 x 181 x 124 mm (1.53" x 7.13" x 4.88"), 1.4 Kg (3 lb) Summit Z516 Controller: 114 x 20 x 207 mm (4.47" x 0.8" x 8.14"), 1.0 Kg (2 lb)
Power Requirements	90 - 264 VAC, 47 - 63 Hz, 221W
Environmental	Temperature (operating): 5° to 40°C (41° to 104°F) Temperature (non-operating): -20° to 60°C (-4° to 140° F) Humidity (operating): 5% to 80% RH (non-condensing) at <=30°C, 50% max RH (non-condensing) at 40°C Humidity (non-operating): 5% to 95% max RH (non-condensing)

Ordering Information

Product Description

Summit Z516 (licensed as a Gen5 x16 Exerciser)
Summit Z516 (licensed as a Gen5 x8 Exerciser)
Summit Z516 (licensed as a Gen5 x4 Exerciser)
Summit Z516 (licensed as a Gen4 x16 Exerciser)
Summit Z516 (licensed as a Gen4 x8 Exerciser)
Summit Z516 (licensed as a Gen4 x4 Exerciser)

Summit Z516 PCIe IDE/DOE Generation Security Option
PXP-500 G5 DVT Platform
Base PCIe Software License for Summit Z516
CXL Exerciser/Generation Option License

Product Code

PE109AGA-X
PE108AGA-X
PE107AGA-X
PE106AGA-X
PE105AGA-X
PE100AGA-X

PE386SUA-A
PXP-500A-X
PE385SUA-A
PE370SUA-A



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