

Summit™ Z58

PCI Express® 5.0

Protocol Exerciser/Analyzer



Product Capabilities

Exerciser

- x1 to x8 link width
- Data rates to 32 GT/s
- Powerful scripting
- Lane reversal
- Auto-polarity
- Lane scrambling
- Error injection
- Host/Device emulation

Protocol Analysis

- x1 to x8 link width
- LTSSM display
- CATC Trace™ views
- Spreadsheet view
- Trace Expert™ analysis

Key Features

Find errors fast

- One button error check
- Fast upload speed
- Large trace memory
- Powerful triggering/filtering

See and understand the traffic

- Get useful information
- More choices of data views
- More ways to analyze data
- Verification Script Engine

Accurate data capture

- 100% data capture
- x1 to x8 link widths
- Data rates to 32 GT/s

PCIe IDE/DOE Support

Product Development Support for PCI Express 5.0!

The Summit Z58 exerciser/analyzer is designed for developers who need a protocol test system supporting the PCI Express 5.0 specification. Supporting traffic generation at data rates to 32 GT/s with link widths up to 8 lanes, the Summit Z58 is Teledyne LeCroy's latest PCI Express (PCIe®) protocol exerciser, leveraging years of experience in providing advanced protocol test tools to the PCI Express community.

In addition to traffic generation, the system also supports protocol analysis capability, featuring the industry-standard CATC Trace as well as a wide variety of other traffic displays and data reports.

The Summit Z58 supports full traffic generation and device/host emulation, as well as providing the industry a platform for development of standardized compliance test suites.

In addition the system provides error injection functions to enable developers to test error recovery routines important to reliable interoperability of PCI Express 5.0 products.

Typical Applications

The Summit Z58 is a critical test and verification tool to assist engineers in development, debug and validation of their PCIe designs (including early stage power-on testing). Because of its rich programmable environment, scripting can be used for full interoperability testing, improving the reliability of systems.

The Summit Z58 can emulate either PCIe root complexes or device endpoints, allowing new designs to be tested against known standards.

A Wealth of Features

Intuitive software controls blend sophisticated traffic generation and analysis capability with ease-of-use, allowing test suites to be rapidly customized to meet specific test requirements. One feature that helps troubleshoot PCIe links is the ability to fully exercise the Link Training & Status State Machine (LTSSM) transitions. The powerful scripting language also allows for the creation of Transaction Layer Packets (TLPs) and Data Link Layer Packets (DLLPs) at PCIe 5.0 data rates of 32 GT/s. Flow Control and ACK/NAK's policies and structures can be defined and generated under user control. Features addressing LTSSM structures include providing bus traffic to emulate all the states of the LTSSM from the Detect state, to the L0 state and maintaining the L0 state between the host and device. The exerciser also supports lane reversal and can control all polarity and scrambling configurations. An important feature to note is that traffic emulation supports dynamic equalization and Skip EQ training and can handle autonomous speed switching between all combinations of speeds. The exerciser also has the capability to perform error injection for training sequences, as well as standard traffic, both at the packet level and on a per lane basis.

Packet fields not explicitly specified by the user are generated automatically (such as packet numbering and CRCs). The configuration space can be emulated for any device including endpoints, bridges and switches. Support for all PCIe 5.0 data rates allows the Summit Z58 to produce test cases that test the device's ability to auto-negotiate data rates with other devices.

In addition, the ability of the Summit Z58 to produce a wide variety of programmed traffic allows the user to introduce controlled error conditions. As an example, a trace file captured in the Analyzer can be exported and used as the basis for a test script, with selected programmed errors introduced at critical stages to test the device's ability to recognize and recover from error conditions. This allows for detailed testing of simple error recovery and complex multiple error conditions, creating more resilient products that perform well even under less than ideal conditions.



Packet 1050	R←	32.0 x8	TLP	Mem	MWr(32)	Length	RequesterID	Tag	Address	1st BE	Last BE	Data	LCRC	Time Delta	Time Stamp	
					010.00000	32	001:00:0	0	DA000000	1111	1111	32 dwords	0x0F39C4DF	4.000 ns	0000 . 000 028 177 000 s	
Packet 1051	R→	32.0 x8	DLLP	ACK	AckNak Seq_Num	CRC 16	Idle	Time Stamp								
					3209	0x2517	30.500 ns	0000 . 000 028 181 000 s								
Packet 1052	R→	32.0 x8	DLLP	UpdateFC-P	HdrScale	HdrFC	DataScale	DataFC	CRC 16	Time Delta	Time Stamp					
					1	218	1	3960	0xB94A	1.000 ns	0000 . 000 028 213 500 s					
Packet 1053	R←	32.0 x8	TLP	Mem	MWr(32)	Length	RequesterID	Tag	Address	1st BE	Last BE	Data	LCRC	Idle	Time Stamp	
					010.00000	32	001:00:0	0	DA000000	1111	1111	32 dwords	0x7B8BA620	2.180 ns	0000 . 000 028 214 500 s	
Packet 1054	R←	32.0 x8	EDS	EDS Symbols	Idle	Time Stamp										
				1F 80 90 00	0.000 ns	0000 . 000 028 254 250 s										
Packet 1055	R←	32.0 x8	SKIP	SKIP Symbols	END	P	FR	SR	CRC	MP	UM	MT	RN	Payload	Idle	Time Stamp
				99 99 99 99 99 ...	78	1	1	1	25	0	0	7	0	156	0.000 ns	0000 . 000 028 255 250 s

Protocol Analysis Option

The Summit Z58 can also support up to eight (8) lanes of protocol analysis. Using its high speed trace memory (up to 8 GB), the Summit Z58 can monitor, capture, decode and analyze PCIe protocols with data rates up to 32GT/s (PCIe 5.0). The application display is highly configurable and can be modified to most users' debugging styles. Many features are available including a hierarchical display, protocol traffic summaries, detailed error reports, timing calculators, bus utilization graphs, and the ability to create user-defined test reports allowing developers to troubleshoot intricate problems and finish their projects on time.

PCIe storage decodes such as NVMe, SATA Express (AHCI and ATA), SCSI Express (PQI and SOP), TCG (Trusted Computing Group), Precision Time Measurement (PTM) and virtualization decodes such as Single and Multi-Root I/O Virtualization (SRIOV and MRIOV) as well as Address Translation Services (ATS) are available to broaden its capabilities to many different industry segments.



Specifications

Host Machine Minimum Requirements	64-bit (x64) versions of Windows® 11, Windows 10, Windows Server 2016, and Windows Server 2019. o The latest Service Pack available for the Windows OS in use is required. 4 GB of RAM; storage with at least 2 GB of free space for the installation of the software and additional space for recorded data; display with resolution of at least 1024x768 with at least 16-bit color depth; USB 2.0/3.0/3.1 port and/ or 100/1000 Mbps Ethernet network interface. For optimal performance, please refer to our recommended configuration in the product documentation.
Recording Memory Size	Up to 8GB
Data Rates Supported	2.5 GT/s, 5 GT/s, 8 GT/s, 16 GT/s and 32 GT/s (PCI Express 5.0)
Ports	Summit Z58 x16 Plug-In Card: Connector cable to Summit Z58 controller Summit Z58 Controller: Connector to Interposer, USB Type-C, 1000BASE-T Ethernet, Sync/Data, DC Power (from supplied adapter)
Display Panel	Eight character alphanumeric display
LEDs	Power LED, Status LED, Trigger LED, Four Data Rate LEDs (2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s), 32 GT/s Activity LEDs (2 per lane—Tx/Rx—for 16 lanes), Training LED
Dimensions and Weight	Summit Z58 Plug-In Card: 39 x 181 x 124 mm (1.53" x 7.13" x 4.87"), 1.4 Kg (3 lb) Summit Z58 Controller: 114 x 20 x 207 mm (4.47" x 0.8" x 8.14"), 1.0 Kg (2 lb)
Power Requirements	90 - 264 VAC, 47 - 63 Hz, 221W
Environmental	Temperature (operating): 5° to 40°C (41° to 104°F) Temperature (non-operating): -20° to 60°C (-4° to 140° F) Humidity (operating): 5% to 80% RH (non-condensing) at <=30°C, 50% max RH (non-condensing) at 40°C Humidity (non-operating): 5% to 95% max RH (non-condensing)

Ordering Information

Product Description

Summit Z58 (licensed as a Gen5 x8 Exerciser)
Summit Z58 (licensed as a Gen5 x4 Exerciser)
Summit Z58 (licensed as a Gen4 x8 Exerciser)
Summit Z58 (licensed as a Gen4 x4 Exerciser)

Summit Z58 PCIe IDE/DOE Generation Security Option
Summit Z58 PCIe IDE/DOE Analysis Security Option

PXP-500 G5 DVT Platform

Product Code

PE104AGA-X
PE103AGA-X
PE102AGA-X
PE101AGA-X

PE360SUA-A
PE361SUA-A

PXP-500A-X



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