

quantumdata Product

Family

M41h Video

Analyzer/Generator Product

Overview



TELEDYNE LECROY
Everywhereyoulook™

Help silicon and product developers bring their next-generation video solutions to market—faster, without interoperability problems and at reduced cost



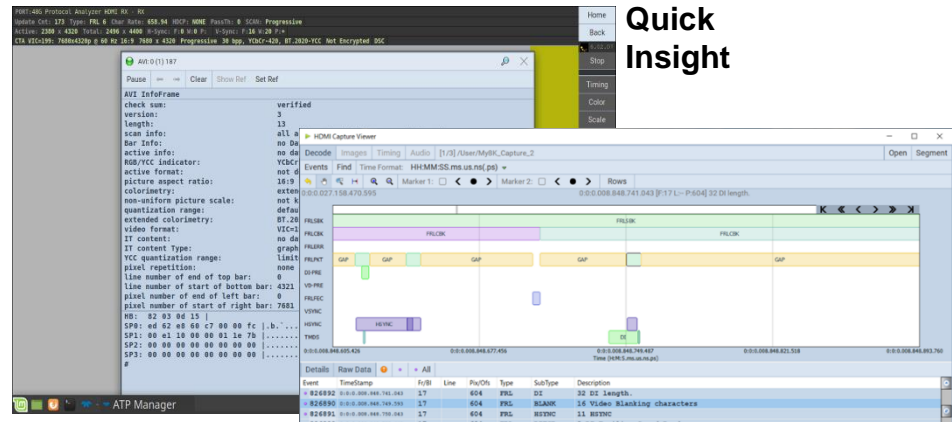
Our solutions quicken Time-to-Insight



What is Time-to-Insight?



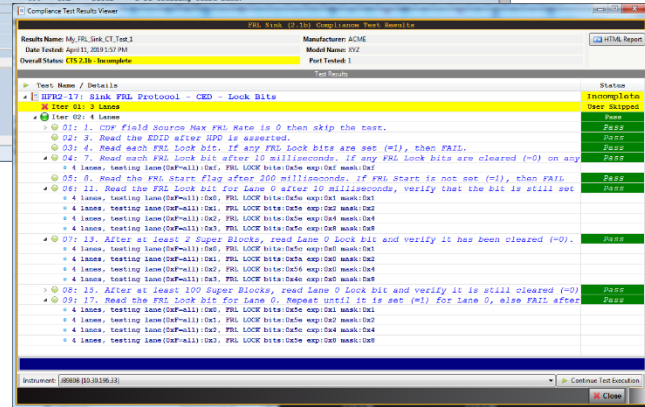
- ◆ **Time-to-Insight saves time and money.** It involves the following:
 - ◆ **Quick Insight:** Provides at-a-glance information—insight—into the basic functioning of an HDMI video device or system.
 - ◆ **Deep Insight:** Provides full visibility—insight—into the low level protocol to verify the proper functioning of an HDMI device to improve interoperability.
 - ◆ **Compliance Tests:** Provides required test suites for HDMI, Logo program.



Quick Insight

Deep Insight

M41h Video Analyzer/Generator



Compliance

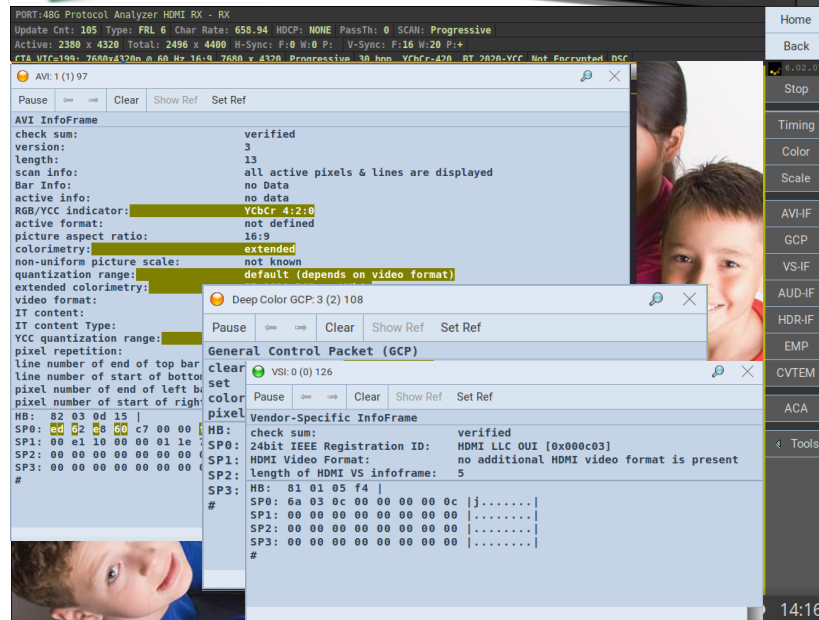
Quick Insight – Example 1

- ◆ Quick Insight Solutions Include:
 - ◆ Real Time analysis views of incoming videos streams.
 - ◆ Essential status information on dashboards, and status panels.
 - ◆ Device emulation of sources and sinks (displays).
- ◆ A Few Examples:
 - ◆ HDMI Real Time view w/ status bar at top. Shows incoming video and metadata from a source device.

HDMI 2.1 source development board



M41h Video Analyzer/Generator

PORT:486 Protocol Analyzer HDMI RX - RX
 Update Cnt: 105 Type: FRL 6 Char Rate: 659.94 HDCP: NONE PassTh: 0 SCAN: Progressive
 Active: 2380 x 4320 Total: 2496 x 4400 H-Sync: F:0 M:0 P: V-Sync: F:16 M:20 P:+
 CTA_VTCr:140-768Hv:320n.6.68 Hz:16.9 7680 x 4320 Progressive 30 hbm VChCr:420 RT 2026-VCC Not Encrypted DSC

AVI:1 (1) 97

AVI InfoFrame
 Check sum: verified
 version: 3
 length: 13
 scan info: all active pixels & lines are displayed
 Bar Info: no data
 active info: no data
 RGB/YCC indicator: YCbCr4:2:0
 active format: not defined
 picture aspect ratio: 16:9
 colorimetry: extended
 non-uniform picture scale: not known
 quantization range: default (depends on video format)
 extended colorimetry:
 video format:
 IT content:
 IT content Type:
 YCC quantization range:
 pixel repetition:
 line number of end of top bar:
 line number of start of bottom bar:
 pixel number of end of left bar:
 pixel number of start of right bar:
 HB: 82 03 0d 15 |
 SP0: 8d 02 58 00 c7 00 00 |
 SP1: 00 e1 10 00 00 01 1e |
 SP2: 00 00 00 00 00 00 00 |
 SP3: 00 00 00 00 00 00 00 |
 #

Deep Color GCP: 3 (2) 108

General Control Packet (GCP)
 vsi: 0 (0) 126

Vendor-Specific InfoFrame
 HB: 81 01 05 f4 |
 SP0: 6a 03 0c 00 00 00 00 0c | j.....|
 SP1: 00 00 00 00 00 00 00 00 ||
 SP2: 00 00 00 00 00 00 00 00 ||
 SP3: 00 00 00 00 00 00 00 00 ||
 #

14:16

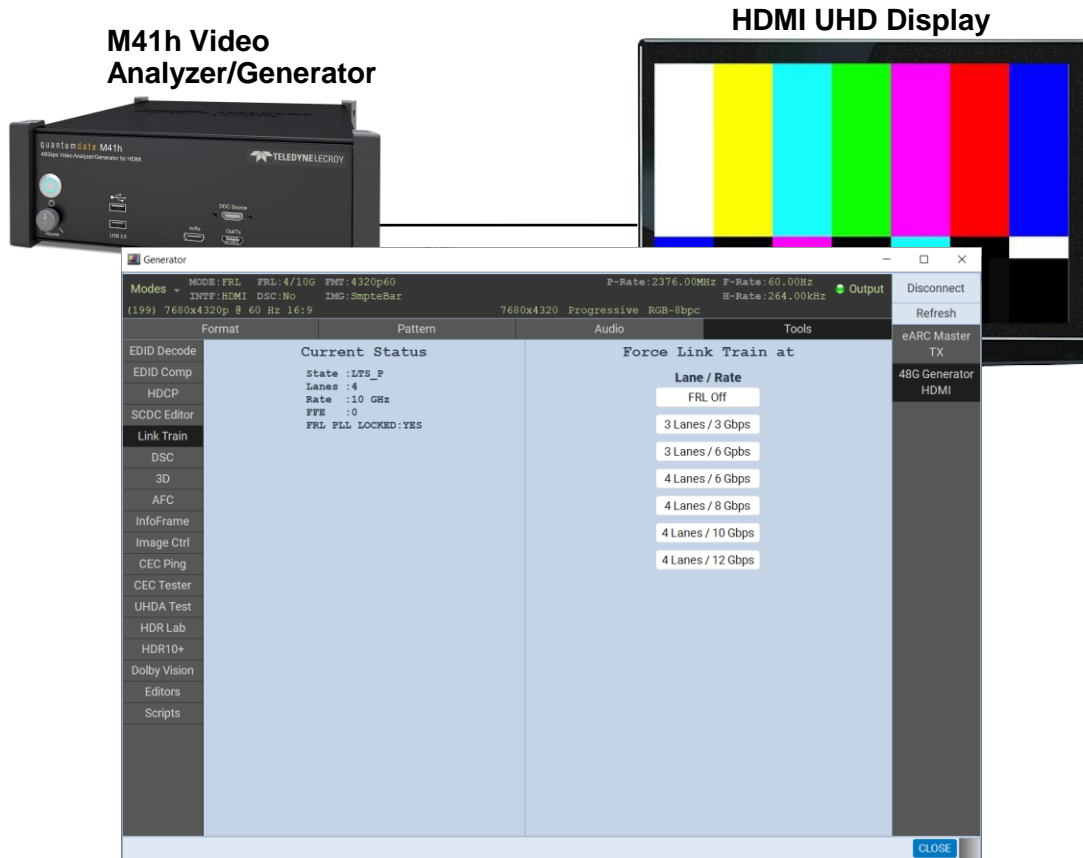
Quick Insight – Example 2

◆ Quick Insight Solutions Include:

- ◆ Real Time analysis views of incoming videos streams.
- ◆ Essential status information on dashboards, and status panels.
- ◆ Device emulation of sources and sinks (displays).

◆ A Few Examples:

- ◆ HDMI FRL link training control & status with connected display.



Quick Insight – Example 3

◆ Quick Insight Solutions Include:

- ◆ Real Time analysis views of incoming videos streams.
- ◆ Essential status information on dashboards, and status panels.
- ◆ Device emulation of sources and sinks (displays).

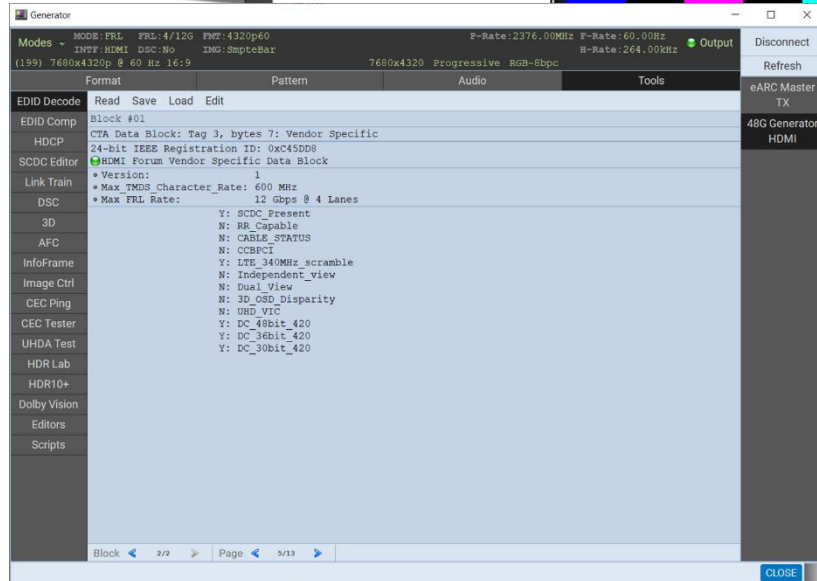
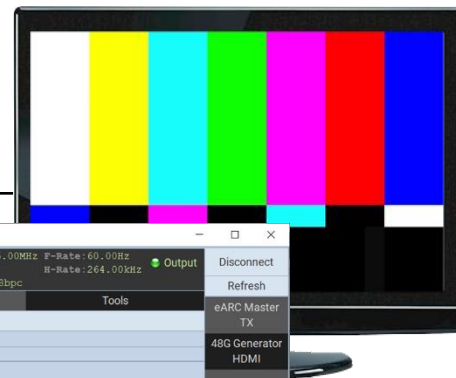
◆ A Few Examples:

- ◆ HDMI EDID and SCDC data view of connected sink device.

M41h Video Analyzer/Generator



HDMI UHD TV



Deep Insight – Example 1

◆ Deep Insight offers:

- ◆ In depth analysis of the low level protocol operation over the main video transmission link.
- ◆ Analysis of connection sequence protocol transactions over the auxiliary channel.

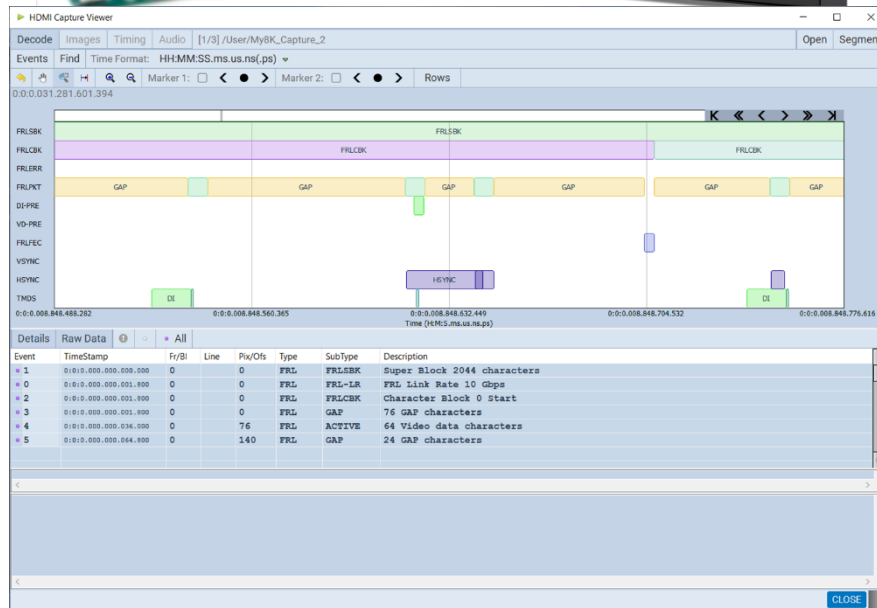
◆ A Few Examples:

- ◆ HDMI capture & analysis of HDMI 2.1 Fixed Rate Link (FRL) transmission providing full visibility into the FRL and TMDS protocol stream.

HDMI 2.1 source development board



M41h Video Analyzer/Generator



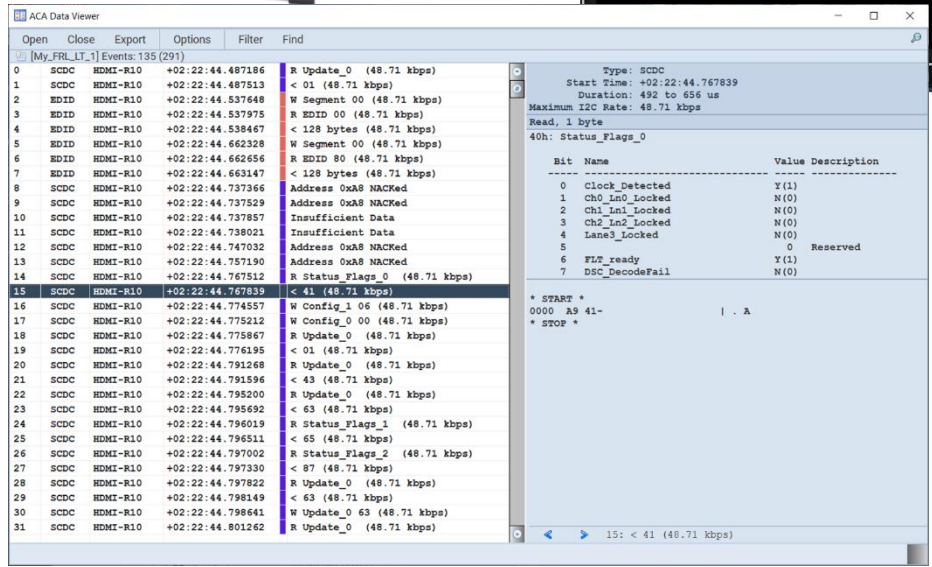
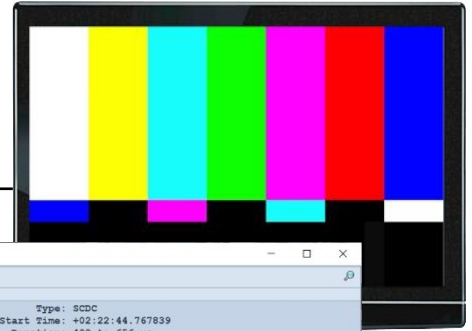
Deep Insight – Example 2

- ◆ Deep Insight offers:
 - ◆ In depth analysis of the low level protocol operation over the main video transmission link.
 - ◆ Analysis of connection sequence protocol transactions over the auxiliary channel.
- ◆ A Few Examples:
 - ◆ Analysis of HDMI 2.1 FRL Link Training transactions.

M41h Video Analyzer/Generator



HDMI UHD TV



The screenshot shows the ACA Data Viewer interface with a list of transactions and a detailed view of a selected event.

Index	Type	Channel	Time	Event	Rate
0	SCDC	HDMI-R10	+02:22:44.487186	R Update_0	48.71 kbps
1	SCDC	HDMI-R10	+02:22:44.487513	< 01	48.71 kbps
2	EDID	HDMI-R10	+02:22:44.537648	W Segment 00	48.71 kbps
3	EDID	HDMI-R10	+02:22:44.537975	R EDID 00	48.71 kbps
4	EDID	HDMI-R10	+02:22:44.538467	< 128 bytes	48.71 kbps
5	EDID	HDMI-R10	+02:22:44.662328	W Segment 00	48.71 kbps
6	EDID	HDMI-R10	+02:22:44.662656	R EDID 80	48.71 kbps
7	EDID	HDMI-R10	+02:22:44.663147	< 128 bytes	48.71 kbps
8	SCDC	HDMI-R10	+02:22:44.737366	Address OxA8 NACKed	
9	SCDC	HDMI-R10	+02:22:44.737529	Address OxA8 NACKed	
10	SCDC	HDMI-R10	+02:22:44.737857	Insufficient Data	
11	SCDC	HDMI-R10	+02:22:44.738021	Insufficient Data	
12	SCDC	HDMI-R10	+02:22:44.747032	Address OxA8 NACKed	
13	SCDC	HDMI-R10	+02:22:44.757190	Address OxA8 NACKed	
14	SCDC	HDMI-R10	+02:22:44.767512	R Status_Flags_0	48.71 kbps
15	SCDC	HDMI-R10	+02:22:44.767839	< 41	48.71 kbps
16	SCDC	HDMI-R10	+02:22:44.774557	W Config_1 06	48.71 kbps
17	SCDC	HDMI-R10	+02:22:44.775212	W Config_0 00	48.71 kbps
18	SCDC	HDMI-R10	+02:22:44.775867	R Update_0	48.71 kbps
19	SCDC	HDMI-R10	+02:22:44.776195	< 01	48.71 kbps
20	SCDC	HDMI-R10	+02:22:44.791268	R Update_0	48.71 kbps
21	SCDC	HDMI-R10	+02:22:44.791596	< 43	48.71 kbps
22	SCDC	HDMI-R10	+02:22:44.795200	R Update_0	48.71 kbps
23	SCDC	HDMI-R10	+02:22:44.795692	< 63	48.71 kbps
24	SCDC	HDMI-R10	+02:22:44.796019	R Status_Flags_1	48.71 kbps
25	SCDC	HDMI-R10	+02:22:44.796511	< 65	48.71 kbps
26	SCDC	HDMI-R10	+02:22:44.797002	R Status_Flags_2	48.71 kbps
27	SCDC	HDMI-R10	+02:22:44.797330	< 87	48.71 kbps
28	SCDC	HDMI-R10	+02:22:44.797822	R Update_0	48.71 kbps
29	SCDC	HDMI-R10	+02:22:44.798149	< 63	48.71 kbps
30	SCDC	HDMI-R10	+02:22:44.798641	W Update_0 63	48.71 kbps
31	SCDC	HDMI-R10	+02:22:44.801262	R Update_0	48.71 kbps

ACA Data Viewer
Open Close Export Options Filter Find

[My_FR1_LT_1] Events: 135 (291)

Type: SCDC
Start Time: +02:22:44.767839
Duration: 492 to 656 us
Maximum I2C Rate: 48.71 kbps
Read, 1 byte
40h: Status_Flags_0

Bit	Name	Value	Description
0	Clock_Detected	Y(1)	
1	Ch0_In0_Locked	N(0)	
2	Ch1_In1_Locked	N(0)	
3	Ch2_In2_Locked	N(0)	
4	Lane3_Locked	N(0)	
5		0	Reserved
6	FLL_ready	Y(1)	
7	Disc_DecodeFail	N(0)	

* START *
0000 A9 41- | . . A
* STOP *

15: < 41 (48.71 kbps)

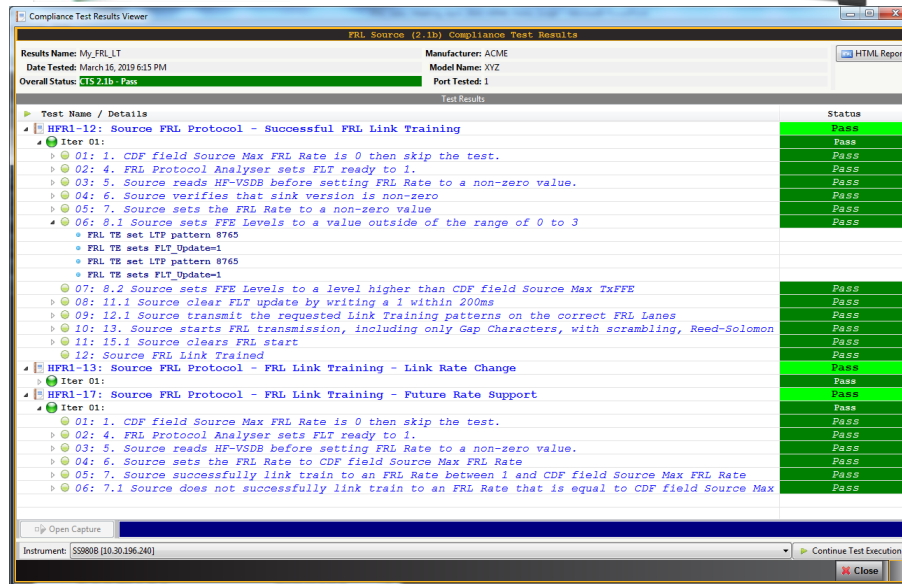
HDMI Compliance Tests – Example 1

- ◆ Compliance Testing Provides:
 - ◆ Required test suites to obtain industry logo.
 - ◆ Detailed test results and logs that provide insight into the cause of failures.
- ◆ A Few Examples:
 - ◆ HDMI 2.1 Fixed Rate Link (FRL) source compliance test suite.

HDMI 2.1 source development board



M41h Video Analyzer/Generator

Compliance Test Results Viewer

FRL Source (2.1b) Compliance Test Results

Results Name: My_FRL_LT Manufacturer: ACME
 Date Tested: March 16, 2019 6:15 PM Model Name: XYZ
 Overall Status: **TS 2.1b - Pass** Port Tested: 1

Test Name / Details	Status
HPRL-12: Source FRL Protocol - Successful FRL Link Training	Pass
Iter 01:	Pass
01: 1. CDF field Source Max FRL Rate is 0 then skip the test.	Pass
02: 4. FRL Protocol Analyser sets FLT ready to 1.	Pass
03: 5. Source reads HF-VSDB before setting FRL Rate to a non-zero value.	Pass
04: 6. Source verifies that sink version is non-zero	Pass
05: 7. Source sets the FRL Rate to a non-zero value	Pass
06: 8.1 Source sets FFE Levels to a value outside of the range of 0 to 3	Pass
FRL TE set LTP pattern 0765	
FRL TE sets FLT_Update=1	
FRL TE set LTP pattern 0765	
FRL TE sets FLT_Update=1	
07: 8.2 Source sets FFE Levels to a level higher than CDF field Source Max TxFFE	Pass
08: 11.1 Source clear FLT update by writing a 1 within 200ms	Pass
09: 12.1 Source transmit the requested Link Training patterns on the correct FRL Lanes	Pass
10: 13. Source starts FRL transmission, including only Gap Characters, with scrambling, Reed-Solomon	Pass
11: 15.1 Source clears FRL start	Pass
12: Source FRL Link Trained	Pass
HPRL-13: Source FRL Protocol - FRL Link Training - Link Rate Change	Pass
Iter 01:	Pass
HPRL-17: Source FRL Protocol - FRL Link Training - Future Rate Support	Pass
Iter 01:	Pass
01: 1. CDF field Source Max FRL Rate is 0 then skip the test.	Pass
02: 4. FRL Protocol Analyser sets FLT ready to 1.	Pass
03: 5. Source reads HF-VSDB before setting FRL Rate to a non-zero value.	Pass
04: 6. Source sets the FRL Rate to CDF field Source Max FRL Rate	Pass
05: 7. Source successfully link train to an FRL Rate between 1 and CDF field Source Max FRL Rate	Pass
06: 7.1 Source does not successfully link train to an FRL Rate that is equal to CDF field Source Max	Pass

Instrument: S508008 (10.30.136.240) Continue Test Execution

HDMI Compliance Tests – Example 2

◆ Compliance Testing Provides:

- ◆ Required test suites to obtain industry logo.
- ◆ Detailed test results and logs that provide insight into the cause of failures.

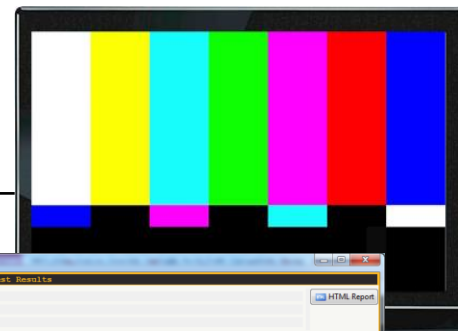
◆ A Few Examples:

- ◆ HDMI sink compliance for Forward Error Correction (FEC).

M41h Video Analyzer/Generator



HDMI FRL UHD Display



Compliance Test Results Viewer

FRL Sink (2.1k) Compliance Test Results

Results Name: AA_NVK_R3_48_Full Manufacturer: qd
 Date Tested: December 11, 2018 11:14 AM Model Name: 900
 Overall Status: **TS 2.1k - f2** Port Tested: 1

Test Name / Details	Status
▶ HFR2-48: Sink FRL Protocol - RS - Basic Operation	Pass
▶ Iter 01: 3 Lanes	Pass
▶ Iter 02: 4 Lanes	Pass
▶ 01: 1. CDF field Source Max FRL Rate is 0 then skip the test.	Pass
▶ 02: 4. Read the RSCC, verify that RS C Valid flag = 0; otherwise FAIL.	Fail
▶ 03: 7. Read each FRL Lock bit. Repeat until all FRL Lock bits are set (=1) on all active Lanes, else FAIL	Pass
▶ 04: 8. Read the FRL Start flag. Repeat until FRL Start is set (=1), else FAIL after 200 milliseconds	Pass
▶ 05: 10. Read the RSCC, verify that RS C Valid flag = 1 and count =0 or 1; otherwise FAIL.	Pass
▶ 06: 11. Corrupt symbols at a rate of about 1e-5, spaced out over 10 seconds, with 1 error/block.	Pass
▶ 07: 12. Read the RSCC; if the value is not correct within 1 count then FAIL.	Pass
▶ 08: 13. Read the RSCC again after 100 milliseconds; if the count is not 0 or 1 then FAIL.	Pass
▶ 09: 14. Corrupt symbols at a rate of about 2e-9, spaced out over 10 seconds, with 2 errors/block in evenly	Pass
▶ 10: 15. Read the RSCC; if the value is not correct within 1 count then FAIL.	Pass
▶ 11: 16. Corrupt one symbol in each of 4 consecutive RS blocks, after generating the RS data	Pass
▶ 12: 17. Change the FRL data stream to be random data on all lanes.	Pass
▶ 13: 18. After 5 seconds, read each FRL Lock bit and verify that they have all been cleared = 0.	Pass
▶ 14: 19. Read the RSCC, verify that RS C Valid flag = 1; otherwise FAIL	Pass
▶ 15: 20. If the count in the RSCC is less than 4, then FAIL.	Pass
▶ HFR2-49: Sink FRL Protocol - RS - Correction Counting During Reads	Fail
▶ Iter 01:	Fail
▶ 01: 1. CDF field Source Max FRL Rate is 0 then skip the test.	Pass
▶ 02: 2. Perform Link Training at the minimum FRL Rate with the maximum number of FRL Lanes supported by the	Pass
▶ 03: 4. Read each FRL Lock bit. Repeat until all FRL Lock bits are set (=1) on all active Lanes, else FAIL	Pass
▶ 04: 7. Read the RSCC, verify that RS C Valid flag = 1 and count =0 or 1; otherwise FAIL.	Pass
▶ 05: 8. Corrupt one symbol in each of a known random number (between 10000 and 30000) of RS blocks over a 1-	Pass
▶ 06: 9. 100 milliseconds after the start of the symbol error, read the RSCC and add the value to a cumulative	Pass
▶ 07: 11.1. If the correction count is outside the range of 12 from the number of generated symbol errors, th	Fail
▶ RS errs 19962 instead of between 19998-20000	Fail
▶ HFR2-50: Sink FRL Protocol - RS - Maximum Symbol Error Count	Pass
▶ HFR2-51: Sink FRL Protocol - RS - Update Flag with Specific Symbol Error Count	Pass
▶ HFR2-52: Sink FRL Protocol - RS - Update Flag with Maximum Symbol Error Count	Pass


HFR2-48: Sink FRL Protocol - RS - Basic Operation

Instrument: PG0808 (10.30.196.17) ▶ Continue Test Execution


HDMI Compliance Tests – Example 3

- ◆ Compliance Testing Provides:
 - ◆ Required test suites to obtain industry logo.
 - ◆ Detailed test results and logs that provide insight into the cause of failures.
- ◆ A Few Examples:
 - ◆ HDCP 2.2 compliance for HDMI source devices.

M41h Video Analyzer/Generator



HDMI 2.1 source



Compliance Test Results Viewer

HDMI HDCP 2.3 TX (1.0) Compliance Test Results

Results Name: AA_HDMI_HDCP_22_PC Manufacturer: Nvidia
Date Tested: May 17, 2016 3:57 PM Model Name: GTX
Overall Status: **GIS 1.0 - fail** Port Tested: 1

Test Results

Test Name / Details	Status
▶ 1A-01: Regular Procedure: With previously connected Receiver (With stored Km)	Pass
▶ 1A-02: Regular Procedure: With newly connected Receiver (Without stored Km)	Pass
▶ 1A-03: Regular Procedure: Receiver disconnect after AKE Init	Pass
Iter 01:	Pass
Clear Ready	
RX HPD Deasserted regular ts:4104052776.96 us	
RX HPD Asserted regular ts:4104202833.92 us	
RX UNAUTH::ENTER	
RX UNAUTH:HDMI/VIDEO Present	
RX UNAUTH:MSG RD:ENC_DIS ts:4104756582.40 us	
RX UNAUTH:MSG RD:VERSION ts:4104756582.40 us	
RX UNAUTH:MSG:Encryption disabled	
RX UNAUTH:RCVD:AKE_Init ts:4105452359.68 us	
RX UNAUTH:**Test Cond.** hpd	
RX HPD Deasserted irregular ts:4105452533.76 us	
RX HPD Asserted irregular ts:4105652561.92 us	
RX UNAUTH:RCVD:AKE_Init ts:4105561569.28 us	
RX UNAUTH:**Test Cond.** ake_init	
RX UNAUTH:Encryption Disabled	
▶ 1A-04: Regular Procedure: Receiver disconnect after Km	Pass
▶ 1A-05: Regular Procedure: Receiver disconnect after locality check	Pass
▶ 1A-06: Regular Procedure: Receiver disconnect after Ks	Fail
Iter 01:	Fail
1A-07: Regular Procedure: Receiver sends REAUTH REQ after Ks	Pass
1A-08: Irregular Procedure: Rx certificate not received.	Pass
1A-09: Irregular Procedure: Verify Receiver Certificate	Pass
1A-01: Regular Procedure: With previously connected Receiver (With stored Km)	

Instrument: S5980B [10.30.196.240] Continue Test Execution

quantumdata M41h Video Analyzer/Generator Test Setups

November - 2019

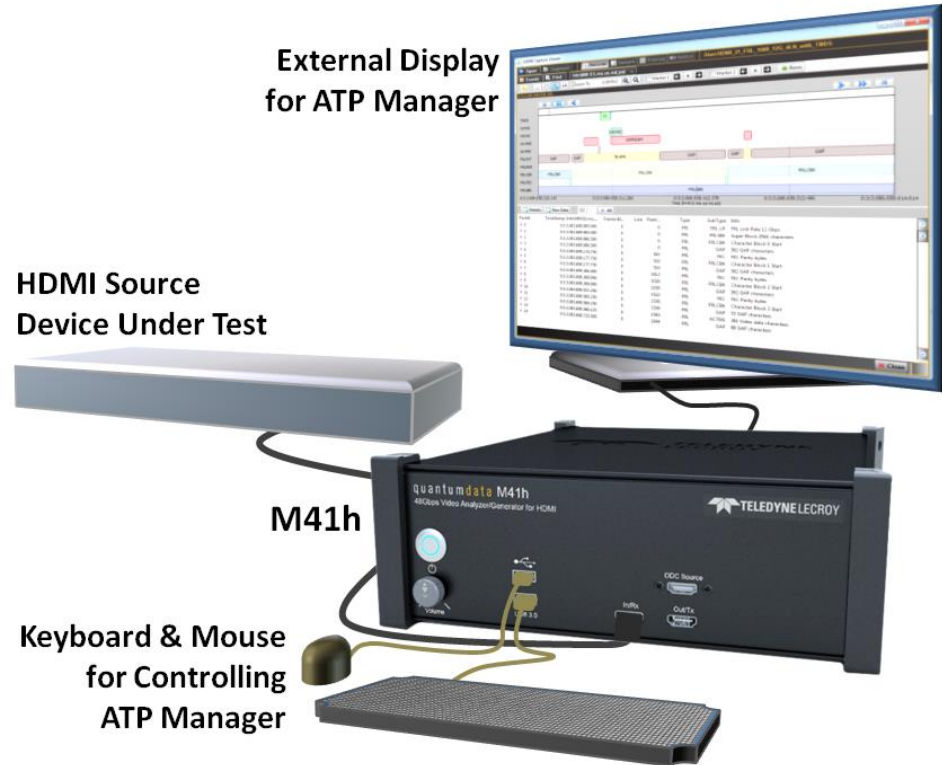


TELEDYNE LECROY
Everywhereyoulook™

M41h Test Setup – HDMI Source Testing

◆ Source testing

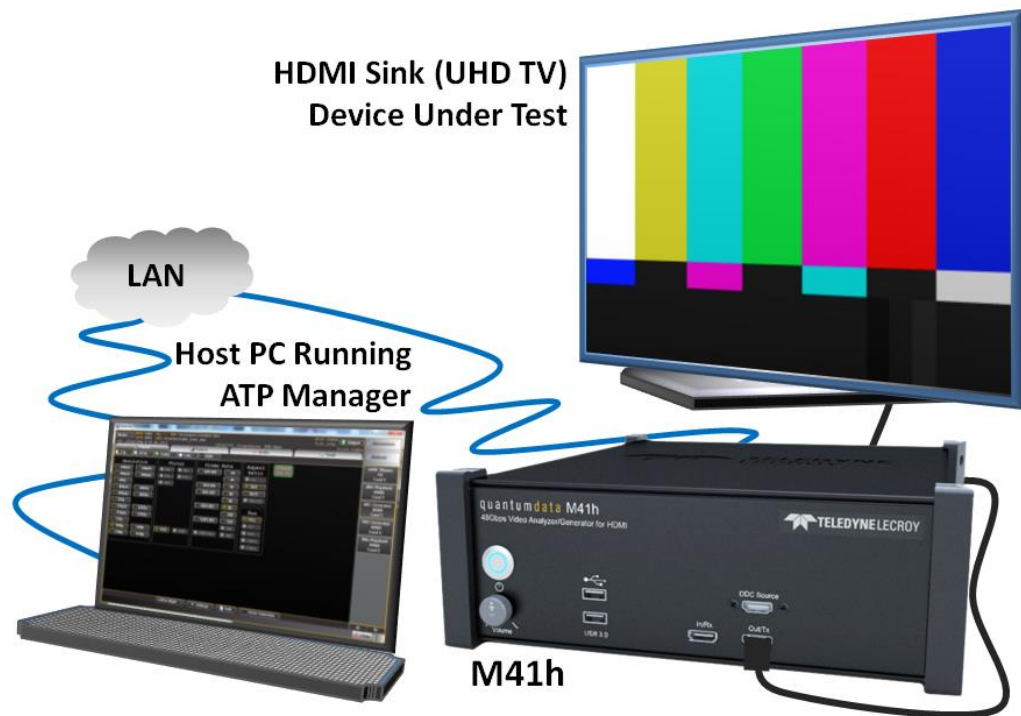
- ◆ Use connected HDCP 2.3 compatible display to view M41h ATP Manager Graphical User Interface.
- ◆ Connection either to DisplayPort or HDMI port on back of M41h.
- ◆ Use Keyboard and mouse to control ATP Manager GUI running on the connected display.



M41h Test Setup – HDMI Sink Testing

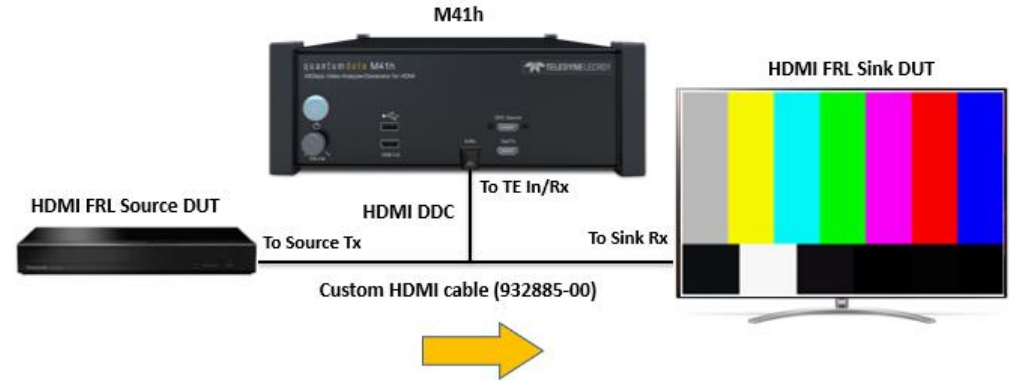
◆ Sink testing

- ◆ Use connected M41h ATP Manager graphical user interface installed on host PC.
- ◆ Use Keyboard and mouse to control ATP Manager GUI running on the connected display.
- ◆ Connect Host PC to M41h via Ethernet cable, either direct or through corporate LAN.



M41h Test Setup – Passive Monitor TMDS and FRL

- ◆ Passive monitoring of DDC channel
 - ◆ You can monitor the DDC channel passively in the **TMDS** mode by connecting a source to the M41h Rx port and a sink to the M41h Tx port.
 - ◆ You can optionally monitor the DDC channel passively in the **FRL** mode using a custom cable.
 - ◆ The DDC passive monitoring enables you to diagnose interoperability problems between a source and a display.
 - ◆ The ability to passively monitor the DDC channel in the FRL mode with the custom cable is especially important for FRL link training and HDCP authentication interoperability.



quantumdata M41h Video Analyzer/Generator Product Details

November - 2019



M41h Video Analyzer / Generator for HDMI 2.1 Testing

- ◆ Provides both Protocol Analysis for FRL / TMDS source testing and Video Generation for FRL / TMDS sink testing.
- ◆ Supports Real Time view of incoming video and essential video parameters.
- ◆ Protocol Analyzer provides deep visibility into the HDMI 2.1 Fixed Rate Link (FRL), FRL with Display Stream Compression (DSC) and TMDS video, audio, metadata, control data and protocol data.
- ◆ Monitors DDC activity: EDID, HDCP and FRL link training with Aux Channel Analyzer (ACA) utility.
- ◆ Video Generator supports HDMI 2.1 FRL and TMDS outputs up to 1485MHz pixel rate for 8K.
- ◆ Supports HDMI 2.1 FRL and TMDS compliance testing for HDMI sources and sinks up to 8K format resolutions.
- ◆ Supports testing of eARC Tx and Rx devices including full compliance testing for both Common mode and Differential mode.



Table of Contents – Link to Sections

◆ Source Testing

- ◆ Real Time Analysis. [→](#)
- ◆ Deep Capture Analysis. [→](#)
- ◆ DDC (Aux Chan) Monitoring. [→](#)
- ◆ FRL and TMDS Compliance. [→](#)
- ◆ HDCP Compliance. [→](#)
- ◆ eARC Rx Testing. [→](#)
- ◆ DDC (Aux Chan) Monitoring. [→](#)
- ◆ Passive DDC Monitoring. [→](#)

◆ Sink Testing

- ◆ Video Generation. [→](#)
- ◆ InfoFrame/Data Island Editing. [→](#)
- ◆ Audio Generation. [→](#)
- ◆ EDID and SCDC. [→](#)
- ◆ FRL and TMDS Compliance. [→](#)
- ◆ HDCP Compliance. [→](#)
- ◆ eARC Tx Testing. [→](#)



HDMI 2.1 Source Testing Real Time Analysis

HDMI Protocol Analyzer – Real Time Analysis

◆ HDMI FRL & TMDS Real Time Analysis:

- ◆ Enables viewing of the incoming video frames.
- ◆ Shows essential video metadata and timing data and FRL link configuration on status bar.

The screenshot displays the HDMI Protocol Analyzer software interface. At the top, a status bar provides technical details: "PORT:48G Protocol Analyzer HDMI RX - RX", "Update Cnt: 89 Type: FRL 6 Char Rate: 658.94 HDCP: NONE PassTh: 0 SCAN: Progressive", "Active: 2380 x 4320 Total: 2496 x 4400 H-Sync: F:0 W:0 P: V-Sync: F:16 W:20 P:+", and "CTA VIC=199: 7680x4320p @ 60 Hz 16:9 7680 x 4320 Progressive 30 bpp, YCbCr-420, BT.2020-YCC Not Encrypted DSC". A yellow arrow points to the "SCAN: Progressive" text. Below the status bar is a large video window showing a group of diverse children smiling and huddled together. To the right of the video window is a vertical navigation menu with buttons for "Home", "Back", "Stop", "Timing", "Color", "Scale", "AVI-IF", "GCP", "VS-IF", "AUD-IF", "HDR-IF", "EMP", "CVTEM", "ACA", and "Tools".

HDMI Protocol Analyzer – Real Time Analysis

HDMI FRL & TMDS Real Time Analysis:

- ◆ Enables viewing of the incoming video frames.
- ◆ Shows essential video metadata and timing data and FRL link configuration on status bar.
- ◆ Shows incoming Display Stream Compression (DSC) frame and indicates if DSC is active.

PORT:486 Protocol Analyzer HDMI RX - RX
Update Cnt: 89 Type: FRL 6 Char Rate: 658.94 HDCP: NONE PassTh: 0 SCAN: Progressi
Active: 2380 x 4320 Total: 2496 x 4400 H-Sync: F:0 W:0 P: V-Sync: F:16 W:20 P:+
CTA VIC-199: 7680x4320p @ 60 Hz 16:9 7680 x 4320 Progressive 30 bpp, YCbCr-420, BT.2020-YCC Not Encrypted DSC

AVI: 1 (1) 97

AVI InfoFrame
check sum: verified
version: 3
length: 13
scan info: all active pixels & lines are displayed
Bar Info: no Data
active info: no data
RGB/YCC indicator: YCbCr 4:2:0
active format: not defined
picture aspect ratio: 16:9
colorimetry: extended
non-uniform picture scale: not known
quantization range: default (depends on video format)
extended colorimetry: BT.2020 RGB or YCbCr
video format: VIC-199 (7680x4320p @ 59.94Hz/60Hz)
IT content: no data
IT content Type: graphics Not used - IT content bit (IT) bit is set to 0
YCC quantization range: limited range
pixel repetition: none
line number of end of top bar: 0
line number of start of bottom bar: 4321
pixel number of end of left bar: 0
pixel number of start of right bar: 7681
HB: 82 03 0d 15 |
SP0: cd 02 00 00 c7 00 00 fc | .b.|...|
SP1: 00 e1 10 00 00 01 1e 7b |{|
SP2: 00 00 00 00 00 00 00 00 ||
SP3: 00 00 00 00 00 00 00 00 ||
#

Protocol Analyzer – Real Time Analysis

◆ HDMI FRL & TMDs Real Time Analysis:

- ◆ Enables viewing of the incoming video frames.
- ◆ Shows essential video metadata and timing data and FRL link configuration on status bar.
- ◆ Provides a real time view of each metadata packet type and the values and change history for each parameter.

PORT:486 Protocol Analyzer HDMI RX - RX
Update Cnt: 105 Type: FRL 6 Char Rate: 658.94 HDCP: NONE PassTh: 0 SCAN: Progressive
Active: 2380 x 4320 Total: 2496 x 4400 H-Sync: F:0 W:0 P: V-Sync: F:16 W:20 P:+
CTA_VTF=199: 7680x4320n @ 60 Hz 16:9 7680 x 4320 Progressive 30 hnn YCbCr-420 RT 2020-YCC Not Encrypted DSC

AVI: 1 (1) 97

Pause Clear Show Ref Set Ref

AVI InfoFrame

check sum: verified
version: 3
length: 13
scan info: all active pixels & lines are displayed
Bar Info: no Data
active info: no data
RGB/YCC indicator: YCbCr 4:2:0
active format: not defined
picture aspect ratio: 16:9
colorimetry: extended
non-uniform picture scale: not known
quantization range: default (depends on video format)
extended colorimetry:
video format:
IT content:
IT content Type:
YCC quantization range:
pixel repetition:
line number of end of top bar:
line number of start of bottom bar:
pixel number of end of left bar:
pixel number of start of right bar:
HB: 82 03 0d 15 |
SP0: e0 02 08 00 c7 00 00 |
SP1: 00 e1 10 00 00 01 1e |
SP2: 00 00 00 00 00 00 00 |
SP3: 00 00 00 00 00 00 00 |
#

Deep Color GCP: 3 (2) 108

Pause Clear Show Ref Set Ref

General Control Packet (GCP)

clear set color pixel

VSI: 0 (0) 126

Vendor-Specific InfoFrame

check sum: verified
SP0: 24bit IEEE Registration ID: HDMI LLC OUI [0x000c03]
SP1: HDMI Video Format: no additional HDMI video format is present
SP2: Length of HDMI VS infoframe: 5
HB: 81 01 05 f4 |
SP0: 6a 03 0c 00 00 00 00 0c | j.....|
SP1: 00 00 00 00 00 00 00 00 |.....|
SP2: 00 00 00 00 00 00 00 00 |.....|
SP3: 00 00 00 00 00 00 00 00 |.....|
#

Home Back Stop Timing Color Scale AVI-IF GCP VS-IF AUD-IF HDR-IF EMP CVTEM ACA Tools 14:16

Protocol Analyzer – Real Time Analysis

◆ HDMI FRL & TMDS Real Time Analysis:

- ◆ Enables viewing of the incoming video frames.
- ◆ Shows essential video metadata and timing data and FRL link configuration on status bar.
- ◆ Provides a real time view of each metadata packet type and the values and change history for each parameter.
- ◆ Emulate a variety of EDIDs and SCDC capability configurations to test an HDMI source's response.

The screenshot shows a software interface for a Protocol Analyzer. At the top, it displays 'PORT:48G Protocol Analyzer HDMI RX - RX' and various system parameters like 'Update Cnt: 105', 'Type: FRL 6', 'Char Rate: 658.94', 'HDCP: NONE', 'PassTh: 0', 'SCAN: Progressive', 'Active: 2380 x 4320', 'Total: 2496 x 4400', 'H-Sync: F:0 W:0 P:', 'V-Sync: F:16 W:20 P:+', 'CTA_VTR=199: 7680x4320n @ 60 Hz 16:9 7680 x 4320 Progressive 30 bpp VChCr=420 RT 2020-Vcr Not Encrypted DSC', and 'AVI: 1 (3) 9514'. A sidebar on the right contains navigation buttons: Home, Back, Stop, Timing, Color, Scale, AVI-IF, GCP, VS-IF, AUD-IF, HDR-IF, EMP, CVTEM, ACA, Tools, and a clock showing 14:16. A central window titled 'Tools: MyM41h (10.30.196.32) 48G Protocol Analyzer HDMI RX - IN/RX' is open, showing a 'Status' button (indicated by a yellow arrow), a 'REFRESH' button (indicated by a yellow arrow), and a list of parameters: State: LTS_P (indicated by a yellow arrow), Lanes: 4, Rate: 10 GHz, MAX_FFE: 0, FLT_NO_TO: 0, FRL_MAX: 0, LTP: 5:6:7:8, Valid GAP Chrs received: YES, Valid Super Block structure: YES, Disparity: lock: CDR Errors, Ln_0: 0:NO:NO, Ln_1: 0:NO:NO, Ln_2: 0:NO:NO, Ln_3: 0:NO:NO, FEC Corrupted Code Block Count: 0, and FEC Symbol Error Count: 0. A 'CLOSE' button is at the bottom right of the window.

Protocol Analyzer – Real Time Analysis with DSC

◆ HDMI FRL & TMDs Real Time Analysis:

- ◆ Enables viewing of the incoming Display Stream Compression (DSC) video frames.
- ◆ Indicates that DSC is active on the status bar.

PORT:48G Protocol Analyzer HDMI RX - RX
Update Cnt: 89 Type: FRL 6 Char Rate: 658.94 HDCP: NONE PassTh: 0 SCAN: Progressive
Active: 2380 x 4320 Total: 2496 x 4400 H-Sync: F:0 W:0 P: V-Sync: F:16 W:20 P:+
CTA VIC=199: 7680x4320p @ 60 Hz 16:9 7680 x 4320 Progressive 30 bpp, YCbCr-4: BT_2020-YCC Not Encrypted DSC

CVTEM: 0 (1) 17

Pause Clear Show Ref Set Ref

CVTEM
PPS Data Bytes: = 128
Version: 1.2
pps_identifier: 0
bits_per_component: 10 bpc
linebuf_depth: 13 bits
block_pred_enable: 1
convert_rgb: 0
simple_422: 0
native_420: 1
native_422: 0
vbr_enable: 0
bits_per_pixel: 238 (7.437500 bits)
pic_height: 4320
pic_width: 7680
slice_height: 4320
slice_width: 1920
chunk_size: 1785
initial_xmit_delay: 275
initial_dec_delay: 995
initial_scale_value: 10
scale_increment_interval: 46304
scale_decrement_interval: 160
first_line_bpg_ofs: 15
nfl_bpg_offset: 8
slice_bpg_offset: 10
initial_offset: 2048
final_offset: 4341
flatness_min_qp: 7
flatness_max_qp: 16
rc_model_size: 8192
rc_edge_factor: 6
rc_quant_incr_limit0: 15
rc_quant_incr_limit1: 15
rc_tgt_offset_hi: 3
rc_tgt_offset_lo: 3
buf_thresh:

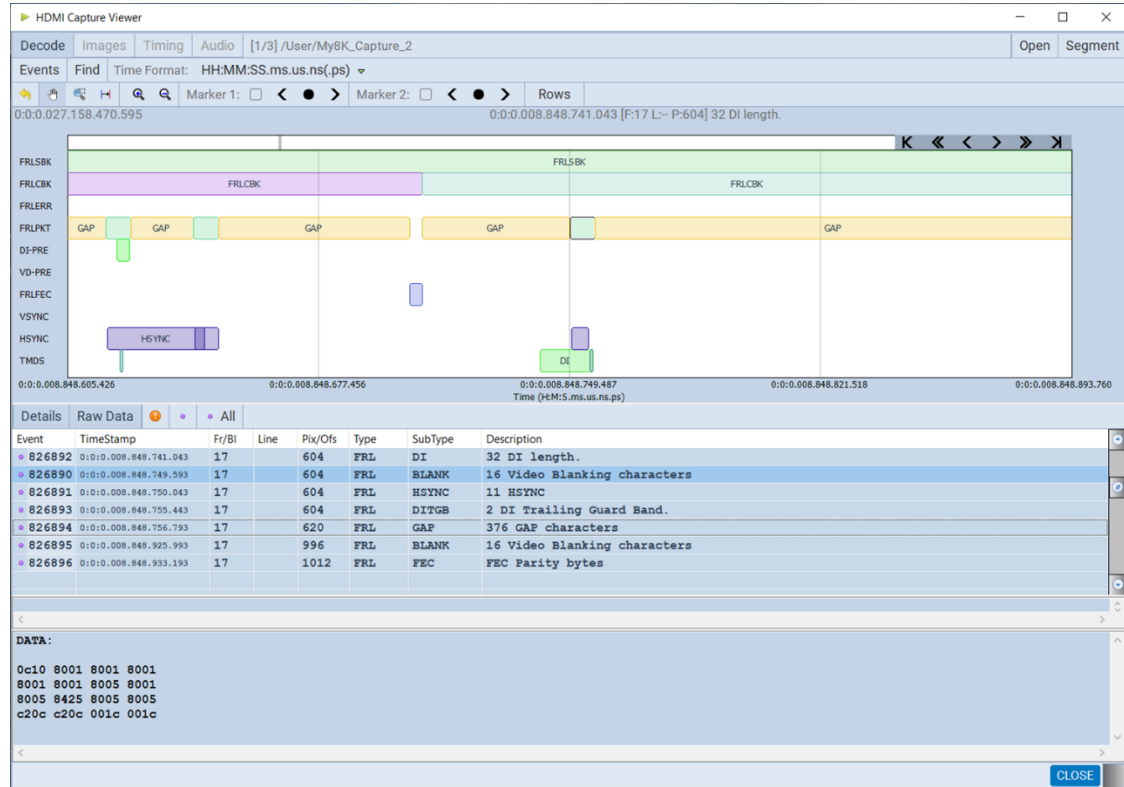
00:	14	28	42	56	70
05:	84	98	105	112	119

HDMI 2.1 Source Testing Capture Analysis

HDMI FRL Protocol Analysis

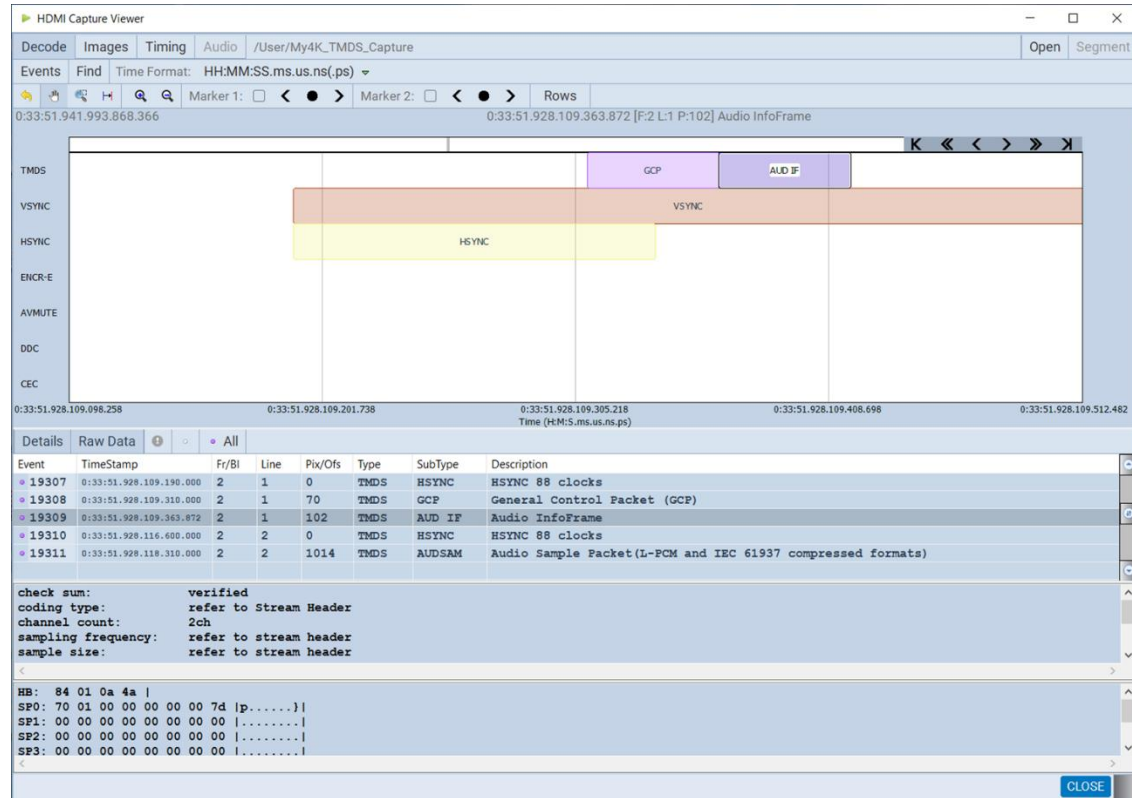
◆ HDMI FRL Capture & Store for Protocol Analysis:

- ◆ Provides graphical view of video, audio, protocol elements in a timeline and in table form.
- ◆ Shows details of all video and protocol elements.
- ◆ Assigns precise timestamps to video / protocol elements.
- ◆ Zoom in and out to get high view or specific view.
- ◆ Provides view of embedded TMDS captured data.
- ◆ Supports searching & filtering of data.
- ◆ Enables export of capture data for sharing with colleagues.
- ◆ View captured video frames.



HDMI TMDS Protocol Capture Analysis

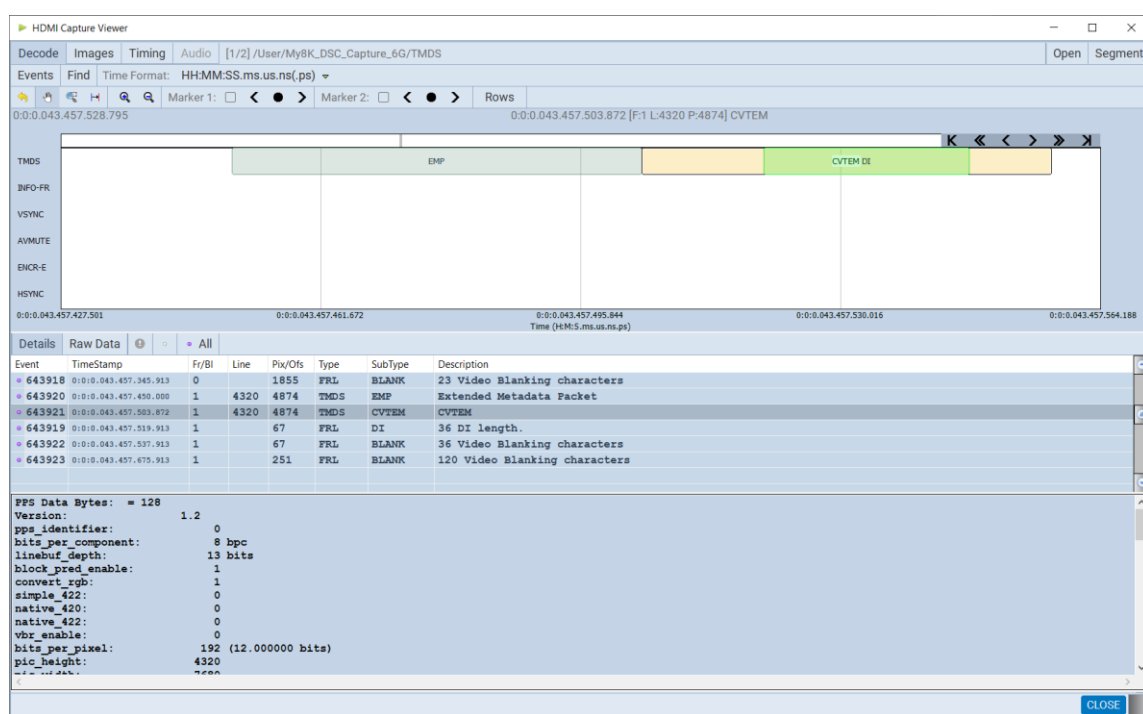
- ◆ HDMI TMDS Capture & Store for Protocol Analysis:
 - ◆ Depicts graphical view of video, audio & protocol elements in a timeline.
 - ◆ TMDS Capture shows details of all video & metadata elements.
 - ◆ Protocol Capture view shows details of low level protocol such as guard bands and preambles.
 - ◆ You can zoom in / out to get a high level view or specific view.
 - ◆ Assigns precise timestamps to video / protocol elements.
 - ◆ Supports search and filtering.
 - ◆ Enables export of capture data for sharing with colleagues.



HDMI TMDS Protocol Capture Analysis - DSC

◆ HDMI TMDS Capture & Store for Protocol Analysis:

- ◆ Depicts graphical view of video, audio & protocol elements in a timeline.
- ◆ TMDS DSC Capture shows details of the video & the DSC metadata, the Picture Parameter Set (PPS) indicated as the CVTEM packet (right).



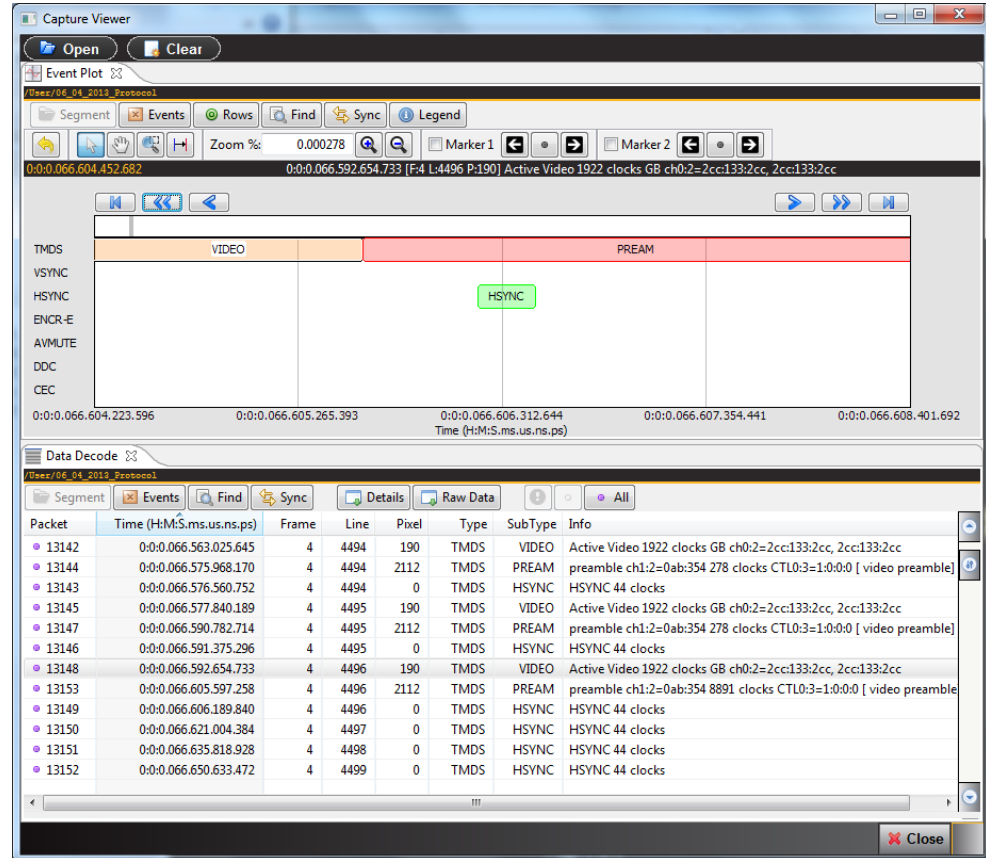
The screenshot displays the HDMI Capture Viewer interface. The main window shows a timeline of captured data with various packets highlighted in different colors. The timeline includes EMP (Extended Metadata Packet) and CVTEM DI (CVTEM Data Interleaved) packets. The details pane at the bottom shows the PPS Data Bytes and parameters.

Event	TimeStamp	Fr/Bt	Line	Pix/Ofs	Type	SubType	Description
643918	0:0:0.043.457.345.913	0	1855	FRL	BLANK		23 Video Blanking characters
643920	0:0:0.043.457.450.000	1	4320	4874	TMDS	EMP	Extended Metadata Packet
643921	0:0:0.043.457.583.872	1	4320	4874	TMDS	CVTEM	CVTEM
643919	0:0:0.043.457.519.913	1		67	FRL	DI	36 DI length.
643922	0:0:0.043.457.537.913	1		67	FRL	BLANK	36 Video Blanking characters
643923	0:0:0.043.457.675.913	1		251	FRL	BLANK	120 Video Blanking characters

PPS Data Bytes: = 128
Version: 1.2
pps_identifier: 0
bits_per_component: 8 bpc
linebuf_depth: 13 bits
block_pred_enable: 1
convert_rgb: 1
simple_422: 0
native_420: 0
native_422: 0
vbr_enable: 0
bits_per_pixel: 192 (12.000000 bits)
pic_height: 4320

HDMI TMDS Protocol Capture Analysis

- ◆ HDMI TMDS Capture & Store for Protocol Analysis:
 - ◆ Depicts graphical view of video, audio & protocol elements in a timeline.
 - ◆ TMDS Capture shows details of all video & metadata elements.
 - ◆ Protocol Capture view shows details of low level protocol such as guard bands and preambles.
 - ◆ You can zoom in / out to get a high level view or specific view.
 - ◆ Assigns precise timestamps to video / protocol elements.
 - ◆ Supports search and filtering.
 - ◆ Enables export of capture data for sharing with colleagues.
 - ◆ Timing analyzer shows Line and Frame timing parameters.



HDMI TMDS Protocol Capture Analysis

◆ HDMI TMDS Capture & Store for Protocol Analysis:

- ◆ Depicts graphical view of video, audio & protocol elements in a timeline.
- ◆ TMDS Capture shows details of all video & metadata elements.
- ◆ Protocol Capture view shows details of low level protocol such as guard bands and preambles.
- ◆ You can zoom in / out to get a high level view or specific view.
- ◆ Assigns precise timestamps to video / protocol elements.
- ◆ Supports search and filtering.
- ◆ Enables export of capture data for sharing with colleagues.
- ◆ Timing analyzer shows Line and Frame timing parameters.

The screenshot shows the 'HDMI Capture Viewer' application. It has tabs for 'Decode', 'Images', 'Timing', and 'Audio'. The current view is 'Timing' for the file '/User/TMDS_4K'. There are 'Open' and 'Segment' buttons in the top right.

Video Format

Format	VIC	BPP	HF (kHz)	I/P	Htotal	Vtotal	Hactive	HS-F	HS-W	VActive	VS-F	VS-W	HS-P	VS-P	HToV	PF (MHz)
2160p60	97	24	135.0	P	4400	2250	3840	176	88	2160	8	44000	Pos	Pos	0	594.0

Frame Statistics

CTA Name	Frame	TimeStamp	Duration	VF Hz	HF kHz	Vtotal	Vactive	PF MHz	HS-W	VSync	Start Vid	HToV	Encr Start	Encr Len	Vfront	Vback
3840x2160p @ 59.94Hz/60Hz	0	0:17:34.618.652.430	0:0:0.016.666.000	60.00	135.00	2250	2160	594.000	88	10	82	0	0	0	8	72
3840x2160p @ 59.94Hz/60Hz	1	0:17:34.635.319.095	0:0:0.016.666.000	60.00	135.00	2250	2160	594.000	88	10	82	0	0	0	8	72
3840x2160p @ 59.94Hz/60Hz	2	0:17:34.651.985.763	0:0:0.016.666.000	60.00	135.00	2250	2160	594.000	88	10	82	0	0	0	8	72
3840x2160p @ 59.94Hz/60Hz	3	0:17:34.668.652.430	0:0:0.016.666.000	60.00	135.00	2250	2160	594.000	88	10	82	0	0	0	8	72
3840x2160p @ 59.94Hz/60Hz	4	0:17:34.685.319.095	0:0:0.016.666.000	60.00	135.00	2250	2160	594.000	88	10	82	0	0	0	8	72
3840x2160p @ 59.94Hz/60Hz	5	0:17:34.701.985.763	0:0:0.016.666.000	60.00	135.00	2250	2160	594.000	88	10	82	0	0	0	8	72

Line Statistics

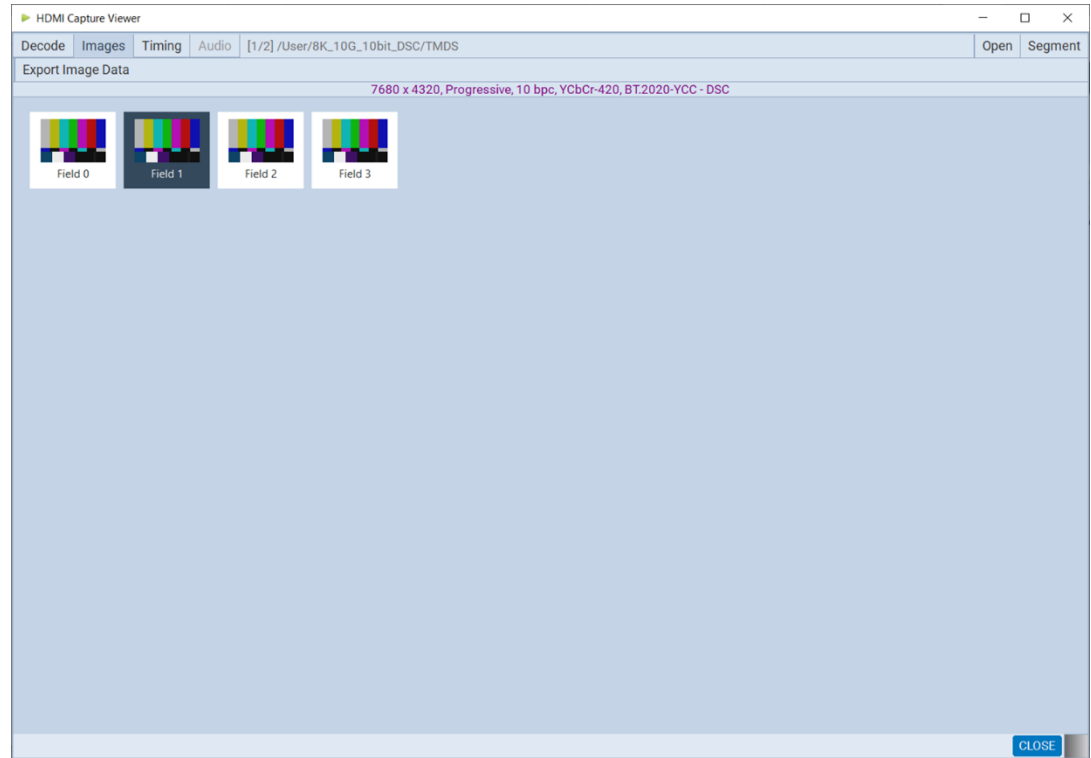
Frame	Line	TimeStamp	Duration	HTotal	TMDS HTotal	HSync Width	HBack	HActive
2	000	0:17:34.651.985.762	0:0:0.000.007.408	4400	4400	88	0	0
2	001	0:17:34.651.993.170	0:0:0.000.007.407	4400	4400	88	0	0
2	002	0:17:34.652.000.577	0:0:0.000.007.408	4400	4400	88	0	0
2	003	0:17:34.652.007.985	0:0:0.000.007.408	4400	4400	88	0	0
2	004	0:17:34.652.015.392	0:0:0.000.007.408	4400	4400	88	0	0
2	005	0:17:34.652.022.800	0:0:0.000.007.407	4400	4400	88	0	0
2	006	0:17:34.652.030.207	0:0:0.000.007.408	4400	4400	88	0	0
2	007	0:17:34.652.037.615	0:0:0.000.007.408	4400	4400	88	0	0
2	008	0:17:34.652.045.022	0:0:0.000.007.408	4400	4400	88	0	0
2	009	0:17:34.652.052.430	0:0:0.000.007.407	4400	4400	88	0	0
2	010	0:17:34.652.059.837	0:0:0.000.007.408	4400	4400	88	0	0
2	011	0:17:34.652.067.245	0:0:0.000.007.405	4400	4400	88	0	0
2	012	0:17:34.652.074.650	0:0:0.000.007.408	4400	4400	88	0	0
2	013	0:17:34.652.082.057	0:0:0.000.007.408	4400	4400	88	0	0
2	014	0:17:34.652.089.465	0:0:0.000.007.408	4400	4400	88	0	0
2	015	0:17:34.652.096.872	0:0:0.000.007.407	4400	4400	88	0	0
2	016	0:17:34.652.104.280	0:0:0.000.007.408	4400	4400	88	0	0
2	017	0:17:34.652.111.687	0:0:0.000.007.408	4400	4400	88	0	0
2	018	0:17:34.652.119.095	0:0:0.000.007.408	4400	4400	88	0	0

A 'CLOSE' button is located in the bottom right corner of the window.

HDMI Capture Viewer – View Captured Video Frames

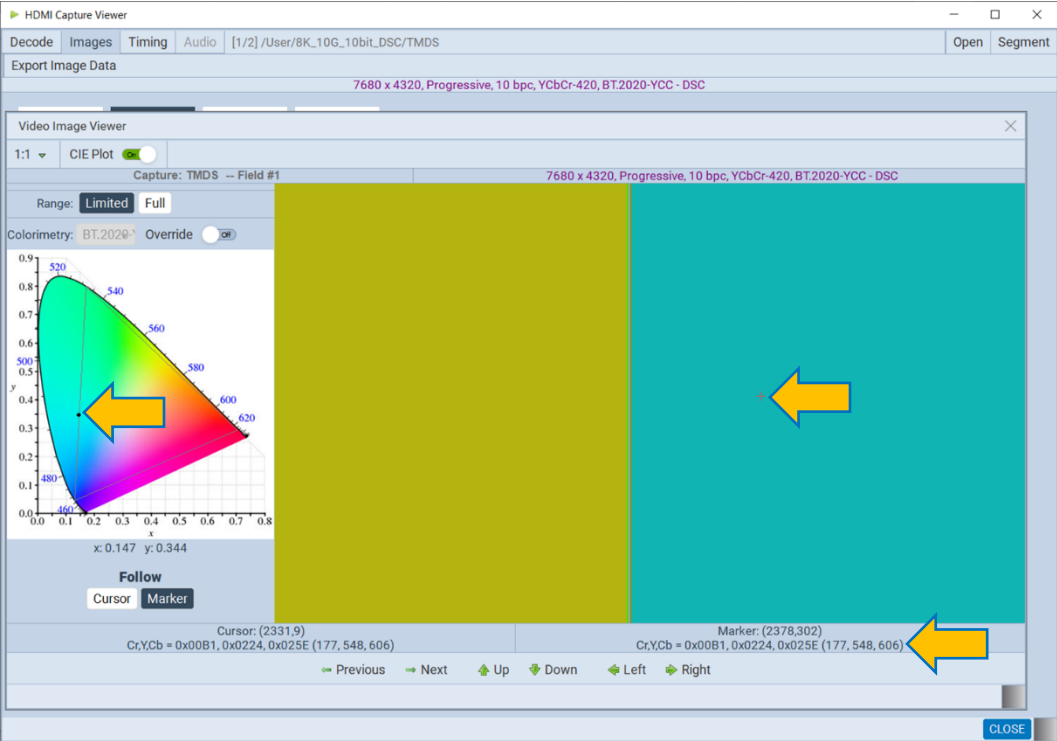
◆ HDMI Capture Viewer Video Frames:

- ◆ View capture video frames to check for artifacts.



HDMI Capture Viewer – View Captured Video Frames

- ◆ HDMI Capture Viewer Video Frames:
 - ◆ View capture video frames to check for artifacts.
 - ◆ Verify colorimetry parameters.
 - ◆ View pixel values.
 - ◆ Check colors against CIE chart.



HDMI Capture Viewer - Searching and Filtering

- ◆ HDMI Capture Viewer Searching and Filtering:
 - ◆ Filter view to show only specific protocol or control elements (example shows audio packets).
 - ◆ View number of packets of each element type for quick at a glance insight into the integrity of the capture.

The screenshot shows the HDMI Capture Viewer interface. At the top, there is a toolbar with a 'Filter' button highlighted by a yellow arrow. Below the toolbar is a waveform display showing TMDs, VSYNC, HSYNC, ENCR-E, AVMUTE, DDC, and CEC signals. A yellow arrow points to the waveform. Below the waveform is a table of events. A yellow arrow points to a specific event in the table. To the right of the table is a 'Decode Event Selection' dialog box. A yellow arrow points to the 'Packets (3947)' category in the dialog box.

Event	TimeStamp	Fr/Bt	Line	Pix/Ofs	Type	SubType	Description
38470	0:17:34.682.259.610.000	4	1837	4262	TMDs	AUDSAM	Audio Sample Pac
38477	0:17:34.682.281.830.000	4	1840	4262	TMDs	AUDSAM	Audio Sample Pac
38484	0:17:34.682.304.050.000	4	1843	4262	TMDs	AUDSAM	Audio Sample Pac
38489	0:17:34.682.318.860.000	4	1845	4262	TMDs	AUDSAM	Audio Sample Pac
38496	0:17:34.682.341.090.000	4	1848	4262	TMDs	AUDSAM	Audio Sample Pac
38503	0:17:34.682.363.310.000	4	1851	4262	TMDs	AUDSAM	Audio Sample Pac
38510	0:17:34.682.385.530.000	4	1854	4262	TMDs	AUDSAM	Audio Sample Pac
38517	0:17:34.682.407.750.000	4	1857	4262	TMDs	AUDSAM	Audio Sample Pac
38523	0:17:34.682.422.940.000	4	1860	86	TMDs	AUDSAM	Audio Sample Pac

HDMI Capture Viewer - Searching and Filtering

HDMI Capture Viewer Searching and Filtering:

- ◆ Filter view to show only specific protocol or control elements (example shows audio packets).
- ◆ Search for any type of video, protocol or control element (example shows searching for a variety of HDMI FRL packets.)
- ◆ View number of packets of each element type for quick at a glance insight into the integrity of the capture.

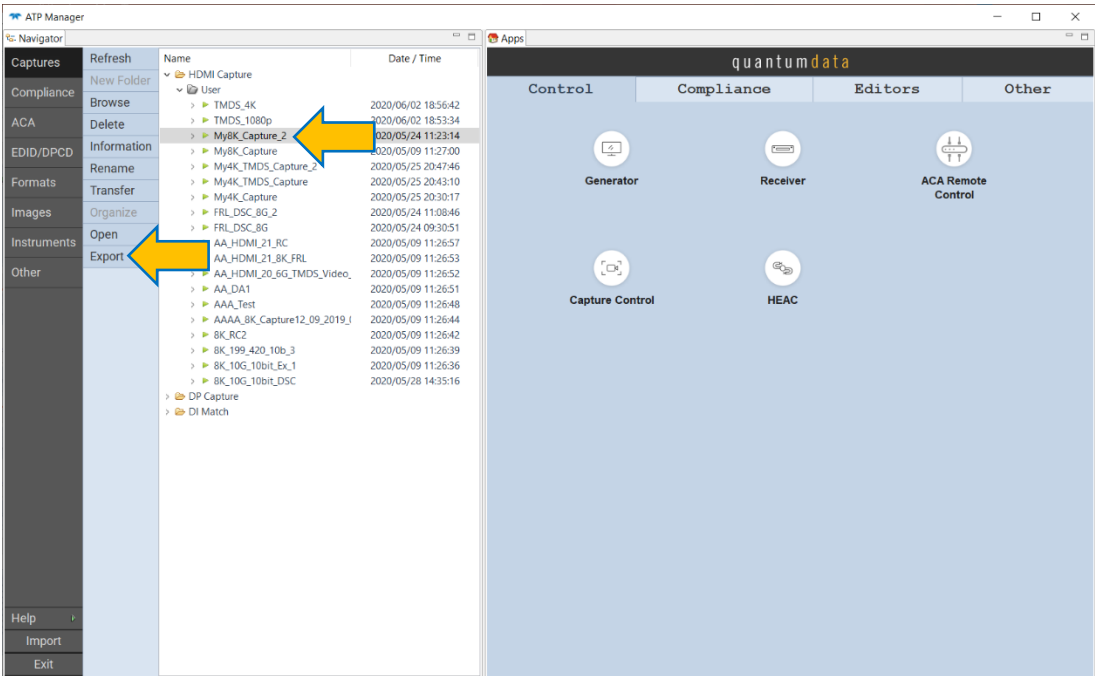
The screenshot shows the HDMI Capture Viewer interface. At the top, there are tabs for Decode, Images, Timing, and Audio. The main window displays a waveform with various signal types: TMDS, VSYNC, HSYNC, INFO-FR, VD-PRE, FRLERR, FRLSKT, FRLPKT, DI-PRE, FRLFEC, and FRLCBK. A yellow arrow points to the FRLSKT signal. A 'Decode Event Selection' dialog box is open, showing a list of event categories and their counts. The 'FRL (3145728)' category is selected. The dialog box has 'Select All' and 'Clear All' buttons. At the bottom of the dialog box, there are buttons for 'SELECT ALL CATEGORIES & EVENTS', 'CLEAR ALL CATEGORIES & EVENTS', 'OK', and 'CANCEL'.

Category	Events
Misc (0)	<input checked="" type="checkbox"/> Link Rate (1)
Packets (0)	<input checked="" type="checkbox"/> Super Block (37662)
InfoFrame (0)	<input checked="" type="checkbox"/> Character Block (150646)
Control (0)	<input checked="" type="checkbox"/> Gap (1439479)
DDC (0)	<input checked="" type="checkbox"/> Active (1316466)
FRL (3145728)	<input checked="" type="checkbox"/> Blank (26347)
Other (0)	<input checked="" type="checkbox"/> FEC Parity (150645)
	<input checked="" type="checkbox"/> FEC Error (0)
	<input checked="" type="checkbox"/> Error (0)
	<input checked="" type="checkbox"/> H-Sync (8023)
	<input checked="" type="checkbox"/> V-Sync (771)
	<input checked="" type="checkbox"/> Encryption Enable (0)
	<input checked="" type="checkbox"/> Video Preamble (4500)
	<input checked="" type="checkbox"/> Video Guard Band (4496)
	<input checked="" type="checkbox"/> Data Island (1673)
	<input checked="" type="checkbox"/> DI Preamble (1673)
	<input checked="" type="checkbox"/> DI Leading GB (1673)
	<input checked="" type="checkbox"/> DI Trailing GB (1673)

HDMI Capture Viewer – Export Capture Data

◆ HDMI Capture Viewer Export:

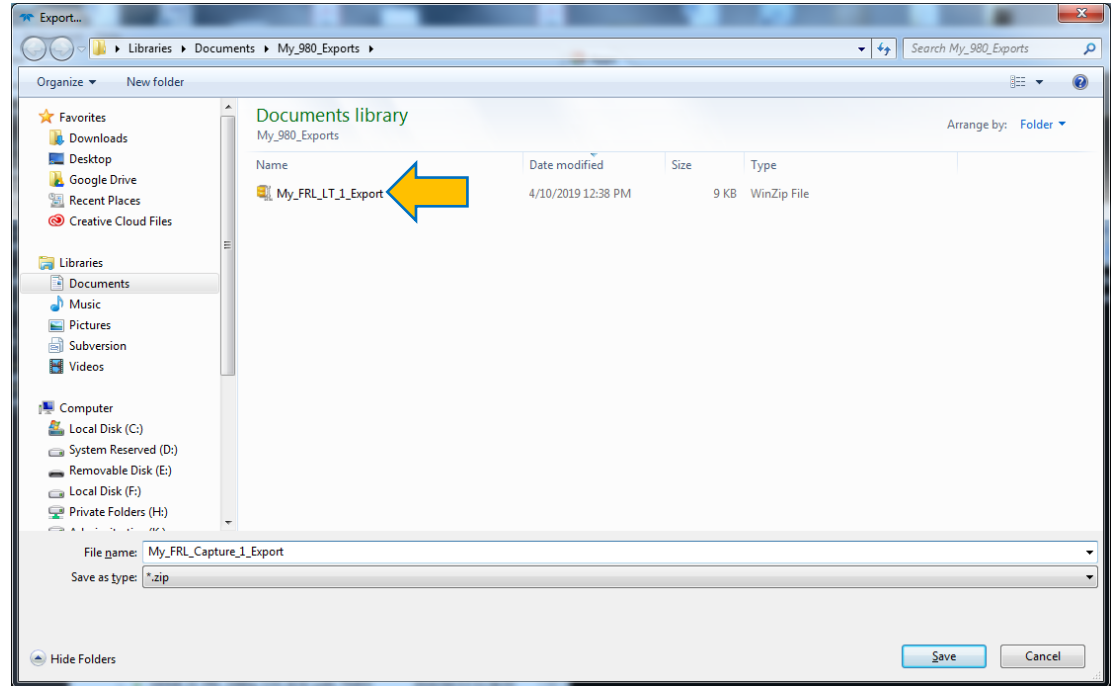
- ◆ Export capture data to disseminate to colleagues, other subject matter experts or Teledyne Customer Support.
- ◆ Exported capture does not require an M41h instrument to view; viewing exported/imported capture only requires ATP Manager which is available on the quantumdata website.



HDMI Capture Viewer – Export Capture Data

◆ HDMI Capture Viewer Export:

- ◆ Export capture data to disseminate to colleagues, other subject matter experts or Teledyne Customer Support.
- ◆ Exported capture does not require an M41h instrument to view; viewing exported/imported capture only requires ATP Manager which is available on the quantumdata website.
- ◆ Transfer to PC to save and recall later for analysis.



HDMI Sink Emulation – Emulate EDIDs and Sink Capability Registers

◆ HDMI EDID and Register Emulation:

- ◆ Create custom EDIDs with the EDID Editor for emulation and verify source response to changing video parameters.
- ◆ Create custom HDMI SCDC register values for emulation and verify source response to link configurations.

EDID Editor

File: /User/FRL-08Gx4L-DSC

APPLY CANCEL

Base Block

- Header
- Vendor/Product Information
- EDID Version/Revision
- Basic Display Parameters/Features
 - Color Characteristics
 - Established Timings
 - Standard Timings
 - Descriptor 1
 - Descriptor 2
 - Descriptor 3
 - Descriptor 4
 - Extension Flag
 - Checksum
- CTA Block
 - Header
- Data Blocks
 - Video Data
 - Audio Data
 - Vendor Specific HDMI 1.4b
 - IEEE OUI: 000C03 (6 Hex Digits)
 - Components of Source Physical Address: 1 0 0 0 0
 - Supports ACP, ISRC1 or ISRC2?
 - Supports 48 bits/pixel (16 bits/color)?
 - Supports 36 bits/pixel (12 bits/color)?
 - Supports 30 bits/pixel (10 bits/color)?
 - Supports YCbCr 4:4:4 in Deep Color modes?
 - Supports DVI dual-link operation?
 - CNC0 - Graphics (text) Supported?
 - CNC1 - Photo Supported?
 - CNC2 - Cinema Supported?
 - CNC3 - Game Supported?
 - Maximum TMDS Clock rate: 340 (5-1275 MHz in steps of 5, 0 = "Not indicated")
 - Audio/Video Latency
 - Range for all values: 0-500 ms
 - Latency fields present?
 - Video Latency: 0 Invalid/Unknown Not Supported
 - Audio Latency: 0 Invalid/Unknown Not Supported
 - Interlaced latency fields present?
 - Interlaced Video Latency: 0 Invalid/Unknown Not Supported
 - Interlaced Audio Latency: 0 Invalid/Unknown Not Supported
 - Video Capability
 - Speaker Allocation
 - YCbCr 4:2:0 Capability Map
 - YCbCr 4:2:0 Video Data
 - HDR Static Metadata
 - Colorimetry
- Detailed Timing Descriptors
- Checksum

Block 1: 128 bytes

Element: Offset = 34, Length = 25

```
02 03 5F F0 59 10 05 20 22 04 03 02 07 4A 78 03 0C 00 10 00 F8 44 2F C8 8A 01 02 4A
5F 60 61 62 64 65 66 C2 C4 C3 76 75 7E 41 00 16 06 08 00 56 58 00
7F 07 F3 03 02 00 10 00 F3 44 2F C8 8A 01 02 4A
04 31 41 00 16 06 08 00 56 58 00 6D D8 1
78 88 47 00 00 00 CF 47 3F E2 00 4B 83 1
E1 0F E4 0E C7 C6 C5 E3 06 0F 01 E3 05 1
00 00 00 00 00 00 00 00 00 00 00 00 00 00 1
00 00 00 00 00 00 00 00 00 00 00 00 00 00 1
```

CLOSE



HDMI DDC Source Testing Aux Channel Analyzer

Aux Channel Analyzer (ACA) – HDMI FRL Link Training

◆ HDMI Aux Channel Analyzer (ACA) for DDC monitoring:

- ◆ Enables monitoring and analysis of the HDMI connection sequence.
- ◆ Verify EDID exchange, HDCP authentication (not shown).
- ◆ View FRL link training transactions.
- ◆ Assigns precise timestamps for each transaction; provides user controls to associate events.
- ◆ Supports search and filtering functions.
- ◆ Enables export of transaction logs to share with colleagues.

ACA Data Viewer

Open Close Export Options Filter Find

AAA_HDMI_48G_FRL_LT Events: 129 (129)

ID	Type	Channel	Timestamp	Data
16	SCDC	HDMI-R30	+00:43:56.475016	< 43 (48.67 kbps)
17	SCDCV	HDMI-R30	+00:43:56.477637	Update Reads 102: 43
18	SCDC	HDMI-R30	+00:43:58.797904	Address 0xA NACKed
19	EDID	HDMI-R30	+00:43:58.847711	W Segment 00 (48.67 kbps)
20	EDID	HDMI-R30	+00:43:58.848202	R EDID 00 (48.67 kbps)
21	EDID	HDMI-R30	+00:43:58.848530	< 128 bytes (48.67 kbps)
22	EDID	HDMI-R30	+00:43:58.978617	W Segment 00 (48.67 kbps)
23	EDID	HDMI-R30	+00:43:58.979108	R EDID 80 (48.67 kbps)
24	EDID	HDMI-R30	+00:43:58.979436	< 128 bytes (48.67 kbps)
25	SCDC	HDMI-R30	+00:43:59.060863	R Sink Version (48.67 kbps)
26	SCDC	HDMI-R30	+00:43:59.061355	< 01 (48.67 kbps)
27	SCDC	HDMI-R30	+00:43:59.061683	W Source Version 01 (48.67 kbps)
28	SCDC	HDMI-R30	+00:43:59.062502	R Status_Flags_0 (48.67 kbps)
29	SCDC	HDMI-R30	+00:43:59.062993	< 41 (48.67 kbps)
30	SCDC	HDMI-R30	+00:43:59.068400	W Config_1 06 (48.67 kbps)
31	SCDC	HDMI-R30	+00:43:59.069055	W Config_0 00 (48.67 kbps)
32	SCDC	HDMI-R30	+00:43:59.069711	R Update_0 (48.67 kbps)
33	SCDC	HDMI-R30	+00:43:59.070202	< 01 (48.67 kbps)
34	SCDC	HDMI-R30	+00:43:59.072660	R Update_0 (48.67 kbps)
35	SCDC	HDMI-R30	+00:43:59.073151	< 01 (48.67 kbps)
36	SCDC	HDMI-R30	+00:43:59.076100	R Update_0 (48.67 kbps)
37	SCDC	HDMI-R30	+00:43:59.076428	< 63 (48.67 kbps)
38	SCDC	HDMI-R30	+00:43:59.076919	R Status_Flags_1 (48.67 kbps)
39	SCDC	HDMI-R30	+00:43:59.077247	< 65 (48.67 kbps)
40	SCDC	HDMI-R30	+00:43:59.077739	R Status_Flags_2 (48.67 kbps)
41	SCDC	HDMI-R30	+00:43:59.078230	< 87 (48.67 kbps)
42	SCDC	HDMI-R30	+00:43:59.078722	R Update_0 (48.67 kbps)
43	SCDC	HDMI-R30	+00:43:59.079049	< 63 (48.67 kbps)
44	SCDC	HDMI-R30	+00:43:59.079541	W Update_0 63 (48.67 kbps)
45	SCDC	HDMI-R30	+00:43:59.082326	R Update_0 (48.67 kbps)
46	SCDC	HDMI-R30	+00:43:59.082654	< 00 (48.67 kbps)
47	SCDCV	HDMI-R30	+00:43:59.085111	Update Reads 52: 00
48	SCDC	HDMI-R30	+00:43:59.232893	R Update_0 (48.67 kbps)
49	SCDC	HDMI-R30	+00:43:59.233384	< 21 (48.67 kbps)

Type: SCDC
Start Time: +00:43:59.068400
Duration: 328 to 492 us
Maximum I2C Rate: 48.67 kbps
Write, 1 byte
31h: Config_1

Bit Name	Value	Description
3-0 FRL_Rate	6	FRL, 12 Gps/lane, 4 Lanes
7-4 FFE_Levels	0	

* START *
0000 A8 31 06 | . . 1 .
* STOP *

30: W Config_1 06 (48.67 kbps)

Aux Channel Analyzer (ACA) – HDMI FRL Link Training

◆ HDMI Aux Channel Analyzer (ACA) Export:

- ◆ Save ACA log as an HTML file.
- ◆ Export capture data to disseminate to colleagues, other subject matter experts or Teledyne Customer Support.
- ◆ Exported capture does not require M41h instrument; only requires ATP Manager.
- ◆ Transfer to PC to save and recall later for analysis.

ACA Data Viewer

Open Close Export Options Filter Find

[AAA_HDMI_48G_FRL_LT] Events: 129 (129)

Time	Channel	Data
44	SCDC HDMI-R30	+00:43:59.079541 W Update_0 63 (48.67 kbps)
45	SCDC HDMI-R30	+00:43:59.082326 R Update_0 (48.67 kbps)
46	SCDC HDMI-R30	+00:43:59.082654 < 00 (48.67 kbps)
47	SCDCU HDMI-R30	+00:43:59.085111 Update Reads 52: 00
48	SCDC HDMI-R30	+00:43:59.232893 R Update_0 (48.67 kbps)
49	SCDC HDMI-R30	+00:43:59.233384 < 21 (48.67 kbps)
50	SCDC HDMI-R30	+00:43:59.233876 R Status_Flags_1 (48.67 kbps)
51	SCDC HDMI-R30	+00:43:59.234203 < FF (48.67 kbps)
52	SCDC HDMI-R30	+00:43:59.234695 R Status_Flags_2 (48.67 kbps)
53	SCDC HDMI-R30	+00:43:59.235023 < FF (48.67 kbps)
54	SCDC HDMI-R30	+00:43:59.235678 W Config_0 00 (48.67 kbps)
55	SCDC HDMI-R30	+00:43:59.236333 W Config_0 00 (48.67 kbps)
56	SCDC HDMI-R30	+00:43:59.241904 R Update_0 (48.67 kbps)
57	SCDC HDMI-R30	+00:43:59.242231 < 21 (48.67 kbps)
58	SCDC HDMI-R30	+00:43:59.242723 W Update_0 21 (48.67 kbps)
59	SCDC HDMI-R30	+00:43:59.243378 W Config_1 05 (48.67 kbps)
60	SCDC HDMI-R30	+00:43:59.244197 R Update_0 (48.67 kbps)
61	SCDCU HDMI-R30	+00:43:59.244689 < 00 (48.67 kbps)
62	SCDCU HDMI-R30	+00:43:59.246983 Update Reads 17: 00
63	SCDC HDMI-R30	+00:43:59.295151 R Update_0 (48.67 kbps)
64	SCDC HDMI-R30	+00:43:59.295479 < 01 (48.67 kbps)
65	SCDC HDMI-R30	+00:43:59.297936 R Update_0 (48.67 kbps)
66	SCDC HDMI-R30	+00:43:59.298264 < 21 (48.67 kbps)
67	SCDC HDMI-R30	+00:43:59.298755 R Status_Flags_1 (48.67 kbps)
68	SCDC HDMI-R30	+00:43:59.299083 < 65 (48.67 kbps)
69	SCDC HDMI-R30	+00:43:59.299575 R Status_Flags_2 (48.67 kbps)
70	SCDC HDMI-R30	+00:43:59.299902 < 87 (48.67 kbps)
71	SCDC HDMI-R30	+00:43:59.300394 R Update_0 (48.67 kbps)
72	SCDC HDMI-R30	+00:43:59.300721 < 21 (48.67 kbps)
73	SCDC HDMI-R30	+00:43:59.301213 W Update_0 21 (48.67 kbps)
74	SCDC HDMI-R30	+00:43:59.303834 R Update_0 (48.67 kbps)
75	SCDC HDMI-R30	+00:43:59.304162 < 21 (48.67 kbps)
76	SCDC HDMI-R30	+00:43:59.304654 R Status_Flags_1 (48.67 kbps)
77	SCDC HDMI-R30	+00:43:59.305145 < 00 (48.67 kbps)

Type: SCDC
Start Time: +00:43:59.305145
Duration: 328 to 492 us
Maximum I2C Rate: 48.67 kbps
Read_1 byte
41h: Status_Flags_1

Bit Name	Value	Description
3-0 In0_LTP_req	0	No Pattern Requested
7-4 In1_LTP_req	0	No Pattern Requested

* START *
0000 A9 00-
* STOP *

77: < 00 (48.67 kbps)

Aux Channel Analyzer (ACA) – HDCP 2.3 Authentication

- ◆ HDMI Aux Channel Analyzer (ACA) for DDC monitoring:
 - ◆ Enables monitoring and analysis of the HDMI connection sequence.
 - ◆ Verify EDID exchange, HDCP authentication.

The screenshot displays the ACA Data Viewer interface with a list of events and a detailed view of a selected event. The event list shows various HDCP messages and their durations. Two yellow arrows highlight specific events: one pointing to 'AKE_Send_Cert (82.61 kbps)' at 00:49:36.098030, and another pointing to 'AKE_No_Stored_km (73.91 kbps)' at 00:49:36.349029.

Time	Protocol	Channel	Direction	Duration	Message	Rate
120	HDCP	HDMI-R10	R	00:49:31.876756	R RxStatus	(73.91 kbps)
121	HDCP	HDMI-R10	<	00:49:31.877084	< 0000	(82.33 kbps)
122	EDID	HDMI-R10	W	00:49:32.368433	W Segment 00	(73.80 kbps)
123	EDID	HDMI-R10	R	00:49:32.368597	R EDID 00	(73.80 kbps)
124	EDID	HDMI-R10	<	00:49:32.368924	< 128 bytes	(82.61 kbps)
125	EDID	HDMI-R10	W	00:49:32.399562	W Segment 00	(73.80 kbps)
126	EDID	HDMI-R10	R	00:49:32.399890	R EDID 80	(73.80 kbps)
127	EDID	HDMI-R10	<	00:49:32.400217	< 128 bytes	(82.61 kbps)
128	HDCP	HDMI-R10	R	00:49:36.027743	R HDCP2Version	(73.69 kbps)
129	HDCP	HDMI-R10	<	00:49:36.028071	< 04	(82.33 kbps)
130	HDCP	HDMI-R10	R	00:49:36.033641	R RxStatus	(73.80 kbps)
131	HDCP	HDMI-R10	<	00:49:36.033805	< 0000	(82.33 kbps)
132	HDCP	HDMI-R10	W	00:49:36.040850	W AKE_Init	(73.91 kbps)
133	HDCP	HDMI-R10	R	00:49:36.096719	R RxStatus	(73.80 kbps)
134	HDCP	HDMI-R10	<	00:49:36.096883	< 1602	(82.47 kbps)
135	HDCP	HDMI-R10	R	00:49:36.097702	R Read_Message	(73.80 kbps)
136	HDCP	HDMI-R10	<	00:49:36.098030	< AKE_Send_Cert	(82.61 kbps)
137	HDCP	HDMI-R10	W	00:49:36.349029	W AKE_No_Stored_km	(73.91 kbps)
138	HDCP	HDMI-R10	R	00:49:36.565786	R RxStatus	(73.80 kbps)
139	HDCP	HDMI-R10	<	00:49:36.566113	< 2100	(82.47 kbps)
140	HDCP	HDMI-R10	R	00:49:36.566933	R Read_Message	(73.80 kbps)
141	HDCP	HDMI-R10	<	00:49:36.567260	< AKE_Send_H_prime	(82.47 kbps)
142	HDCP	HDMI-R10	R	00:49:36.621490	R RxStatus	(73.80 kbps)
143	HDCP	HDMI-R10	<	00:49:36.621818	< 1100	(82.47 kbps)
144	HDCP	HDMI-R10	R	00:49:36.622637	R Read_Message	(73.80 kbps)
145	HDCP	HDMI-R10	<	00:49:36.622965	< AKE_Send_Pairing_Info	(82.47 kbps)
146	HDCP	HDMI-R10	W	00:49:36.637219	W LC_Init	(73.80 kbps)
147	HDCP	HDMI-R10	R	00:49:36.659173	R RxStatus	(73.69 kbps)
148	HDCP	HDMI-R10	<	00:49:36.659337	< 2100	(82.47 kbps)
149	HDCP	HDMI-R10	R	00:49:36.660156	R Read_Message	(73.80 kbps)
150	HDCP	HDMI-R10	<	00:49:36.660484	< LC_Send_L_prime	(82.47 kbps)
151	HDCP	HDMI-R10	W	00:49:36.672280	W SKE_Send_Eks	(73.91 kbps)
152	HDCP	HDMI-R10	R	00:49:36.879371	R RxStatus	(73.80 kbps)
153	HDCP	HDMI-R10	<	00:49:36.879698	< 0000	(82.47 kbps)
154	HDCP	HDMI-R10	R	00:49:37.080563	R RxStatus	(73.69 kbps)
155	HDCP	HDMI-R10	<	00:49:37.080727	< 0000	(82.47 kbps)
156	HDCP	HDMI-R10	R	00:49:37.281592	R RxStatus	(73.80 kbps)

Event Details (Selected):

```
Type: HDCP
Start Time: +00:49:36.098030
Duration: 58.982 msec
Maximum I2C Rate: 82.61 kbps
Read, 534 bytes
Register: 80h
Name: Read_Message
Message: AKE_Send_Cert (534 bytes)
msg_id: 3
cert_rx:[4175..0]
Receiver ID: 8C 23 BA D5 A6
Receiver Public Key:
C5 3B FC EC 4E 2A 42 EA 71 76 F4 B8 90 7A EC
F5 78 07 11 97 35 5C D6 F8 09 30 D3 DB 4C 91
7D 82 CE F6 7D 7F 22 A1 1D A7 9F 6F C1 4A 52
AE 09 5A CC 59 FD 5F C2 07 19 D8 A7 02 D0 4C
B8 16 F4 DA 3A 12 B8 00 84 E1 D3 2E 2C EA 76
83 F8 12 B0 74 E6 B9 CB 5B BD BB F8 39 A3 26
DF B9 E9 5A BD 0F 97 89 73 63 38 2B 95 1D 52
CA 1F 07 46 F1 14 36 1A 3F 61 BE 2E C2 E2 75
01 00 01
RESERVED: 00 00
DCP LLC Signature:
28 A8 50 53 80 72 16 76 A3 EB 07 D7 FC F7 A7
38 72 33 D5 26 76 87 64 3A D1 A4 45 45 86 6D
90 58 B4 3E 16 CD F8 B7 24 D7 74 F9 4E 76 C5
1B D0 E8 4B 53 33 1A 6D 72 E2 3A 8A 79 FE BC
52 9C 21 8E 4D 9F BA 33 2E BA 8F B4 69 36 C4
DF BC 47 6B 5D 3B 4D 72 62 F3 19 B2 24 B5 EE
4A DF 57 82 1F 03 23 DB DB 41 0B 25 79 28 FE
72 ED 4D 42 1F D8 7F 31 A4 9A 97 97 8E 13 10
0D 00 E8 48 97 71 5E 5C B5 1A F1 86 60 0D BA
CC 9A 2C 40 B8 1B 59 50 7B 2A 0B 4E EF DE C3
FF 9E AD E7 9A 0E FC D2 D2 1C 9E 35 25 5E 2C
F7 CC 4C FE B2 0E C2 56 46 57 9F F5 1A 1A 32
5E E1 58 12 57 48 47 33 96 4C 0B 99 E7 C3 5E
61 80 DD B6 23 BE 3E 97 82 4F 11 B4 70 86 2F
A8 C2 95 C1 F5 EC 39 8F 6C E3 7E F0 13 EE
B2 F0 95 01 A4 74 F2 95 3C 10 9B 5B B9 60 61
BC 9E 0C 07 DA 72 C7 74 B6 15 75 E1 65 A7 BF
88 E7 F0 D9 16 9E 13 D5 8D 96 93 0F 3A E1 0D
```

Aux Channel Analyzer (ACA) – HDCP 2.3 Authentication

- ◆ HDMI Aux Channel Analyzer (ACA) for DDC monitoring:
 - ◆ Enables monitoring and analysis of the HDMI connection sequence.
 - ◆ Verify EDID exchange, HDCP authentication.

The screenshot displays the ACA Data Viewer interface. The main window shows a list of events for the ACMT_HDCP_1B_07_2 connection. The log entries include:

- 120 HDCP HDMI-R10 +00:49:31.876756 R RxStatus (73.91 kbps)
- 121 HDCP HDMI-R10 +00:49:31.877084 < 0000 (82.33 kbps)
- 122 EDID HDMI-R10 +00:49:32.368433 W Segment 00 (73.80 kbps)
- 123 EDID HDMI-R10 +00:49:32.368597 R EDID 00 (73.80 kbps)
- 124 EDID HDMI-R10 +00:49:32.368924 < 128 bytes (82.61 kbps)
- 125 EDID HDMI-R10 +00:49:32.399562 W Segment 00 (73.80 kbps)
- 126 EDID HDMI-R10 +00:49:32.399890 R EDID 80 (73.80 kbps)
- 127 EDID HDMI-R10 +00:49:32.400217 < 128 bytes (82.61 kbps)
- 128 HDCP HDMI-R10 +00:49:36.027743 R HDCP2Version (73.69 kbps)
- 129 HDCP HDMI-R10 +00:49:36.028071 < 04 (82.33 kbps)
- 130 HDCP HDMI-R10 +00:49:36.033641 R RxStatus (73.80 kbps)
- 131 HDCP HDMI-R10 +00:49:36.033805 < 0000 (82.33 kbps)
- 132 HDCP HDMI-R10 +00:49:36.040850 W AKE_Init (73.91 kbps)
- 133 HDCP HDMI-R10 +00:49:36.096719 R RxStatus (73.80 kbps)
- 134 HDCP HDMI-R10 +00:49:36.096883 < 1602 (82.47 kbps)
- 135 HDCP HDMI-R10 +00:49:36.097702 R Read_Message (73.80 kbps)
- 136 HDCP HDMI-R10 +00:49:36.098030 < AKE_Send_Cert (82.61 kbps)
- 137 HDCP HDMI-R10 +00:49:36.349029 W AKE_No_Stored_km (73.91 kbps)
- 138 HDCP HDMI-R10 +00:49:36.565786 R RxStatus (73.80 kbps)
- 139 HDCP HDMI-R10 +00:49:36.566113 < 2100 (82.47 kbps)
- 140 HDCP HDMI-R10 +00:49:36.566933 R Read_Message (73.80 kbps)
- 141 HDCP HDMI-R10 +00:49:36.567260 < AKE_Send_H_prime (82.47 kbps)
- 142 HDCP HDMI-R10 +00:49:36.621490 R RxStatus (73.80 kbps)
- 143 HDCP HDMI-R10 +00:49:36.621818 < 1100 (82.47 kbps)
- 144 HDCP HDMI-R10 +00:49:36.622637 R Read_Message (73.80 kbps)
- 145 HDCP HDMI-R10 +00:49:36.622965 < AKE_Send_Pairing_Info (82.47 kbps)
- 146 HDCP HDMI-R10 +00:49:36.637219 W LC_Init (73.80 kbps)
- 147 HDCP HDMI-R10 +00:49:36.659173 R RxStatus (73.69 kbps)
- 148 HDCP HDMI-R10 +00:49:36.659337 < 2100 (82.47 kbps)
- 149 HDCP HDMI-R10 +00:49:36.660156 R Read_Message (73.80 kbps)
- 150 HDCP HDMI-R10 +00:49:36.660484 < LC_Send_L_prime (82.47 kbps)
- 151 HDCP HDMI-R10 +00:49:36.672280 W SKE_Send_Eks (73.91 kbps)
- 152 HDCP HDMI-R10 +00:49:36.879371 R RxStatus (73.80 kbps)
- 153 HDCP HDMI-R10 +00:49:36.879698 < 0000 (82.47 kbps)
- 154 HDCP HDMI-R10 +00:49:37.080563 R RxStatus (73.69 kbps)
- 155 HDCP HDMI-R10 +00:49:37.080727 < 0000 (82.47 kbps)
- 156 HDCP HDMI-R10 +00:49:37.281592 R RxStatus (73.80 kbps)

The detailed view pane on the right shows the following information for the selected event (137):

- Type: HDCP
- Start Time: +00:49:36.349029
- Duration: 16.220 msec
- Maximum I2C Rate: 73.91 kbps
- Write, 129 bytes
- Register: 60h
- Name: Write_Message
- Message: AKE_No_Stored_km (129 bytes)
- msg_id: 4
- Ekpub_km[1023..0]:
- 38 51 27 27 85 36 1F B6 87 EF F1 4F F7 63 41 1A
- 58 7D 7C B9 C5 34 9E DD 05 A5 F9 5B 01 3A B5 EB
- 48 05 52 11 9A C6 64 93 69 67 47 12 3B C8 10 73
- B1 89 0F D4 D8 57 75 94 B8 60 8E 90 C8 03 D0 1B
- A5 EA 83 2A 70 EC F5 CD 02 5E 32 CB 78 2C 6D 53
- B1 6E AF 5E 60 9F 09 D0 E5 E1 BC C3 12 7D E2 DC
- 84 DB 21 B3 91 16 C4 D8 7A 4D 9A 32 D7 DF 29 B4
- A2 D1 56 D9 FE 41 45 0E 69 AF 31 45 B3 7B 65 8C

Aux Channel Analyzer (ACA) – EDID Exchange HDCP 1.4

◆ HDMI Aux Channel Analyzer (ACA) for DDC monitoring:

- ◆ Enables monitoring and analysis of the HDMI connection sequence.
- ◆ Verify EDID exchange, HDCP authentication transactions.
- ◆ Supports search and filtering functions.
- ◆ Assigns precise timestamps for each transaction; provides user controls to associate events.
- ◆ Enables export of transaction logs to share with colleagues.

The screenshot displays the ACA Data Viewer interface. The main window shows a list of events with columns for time, protocol, channel, and data. A yellow arrow points to the event at timestamp +00:49:32.400217, which is an EDID transaction. The right-hand pane provides a detailed view of this EDID, including its start time, duration, maximum I2C rate, and the raw data bytes.

Time	Protocol	Channel	Data
120	HDCP	HDMI-R10	+00:49:31.876756 R RxStatus (73.91 kbps)
121	HDCP	HDMI-R10	+00:49:31.877084 < 0000 (82.33 kbps)
122	EDID	HDMI-R10	+00:49:32.368433 W Segment 00 (73.80 kbps)
123	EDID	HDMI-R10	+00:49:32.368597 R EDID 00 (73.80 kbps)
124	EDID	HDMI-R10	+00:49:32.368924 < 128 bytes (82.61 kbps)
125	EDID	HDMI-R10	+00:49:32.399562 W Segment 00 (73.80 kbps)
126	EDID	HDMI-R10	+00:49:32.399890 R EDID 80 (73.80 kbps)
127	EDID	HDMI-R10	+00:49:32.400217 < 128 bytes (82.61 kbps)
128	HDCP	HDMI-R10	+00:49:36.027743 R HDCP2Version (73.69 kbps)
129	HDCP	HDMI-R10	+00:49:36.028071 < 04 (82.33 kbps)
130	HDCP	HDMI-R10	+00:49:36.033641 R RxStatus (73.80 kbps)
131	HDCP	HDMI-R10	+00:49:36.033805 < 0000 (82.33 kbps)
132	HDCP	HDMI-R10	+00:49:36.040850 W AKE_Init (73.91 kbps)
133	HDCP	HDMI-R10	+00:49:36.096719 R RxStatus (73.80 kbps)
134	HDCP	HDMI-R10	+00:49:36.096883 < 1602 (82.47 kbps)
135	HDCP	HDMI-R10	+00:49:36.097702 R Read_Message (73.80 kbps)
136	HDCP	HDMI-R10	+00:49:36.098030 < AKE_Send_Cert (82.61 kbps)
137	HDCP	HDMI-R10	+00:49:36.349029 W AKE_No_stored_km (73.91 kbps)
138	HDCP	HDMI-R10	+00:49:36.565786 R RxStatus (73.80 kbps)
139	HDCP	HDMI-R10	+00:49:36.566113 < 2100 (82.47 kbps)
140	HDCP	HDMI-R10	+00:49:36.566933 R Read_Message (73.80 kbps)
141	HDCP	HDMI-R10	+00:49:36.567260 < AKE_Send_H_prime (82.47 kbps)
142	HDCP	HDMI-R10	+00:49:36.621490 R RxStatus (73.80 kbps)
143	HDCP	HDMI-R10	+00:49:36.621818 < 1100 (82.47 kbps)
144	HDCP	HDMI-R10	+00:49:36.622637 R Read_Message (73.80 kbps)
145	HDCP	HDMI-R10	+00:49:36.622965 < AKE_Send_Pairing_Info (82.47 kbps)
146	HDCP	HDMI-R10	+00:49:36.637219 W LC_Init (73.80 kbps)
147	HDCP	HDMI-R10	+00:49:36.659173 R RxStatus (73.69 kbps)
148	HDCP	HDMI-R10	+00:49:36.659337 < 2100 (82.47 kbps)
149	HDCP	HDMI-R10	+00:49:36.660156 R Read_Message (73.80 kbps)
150	HDCP	HDMI-R10	+00:49:36.660484 < LC_Send_L_prime (82.47 kbps)
151	HDCP	HDMI-R10	+00:49:36.672280 W SKE_Send_Eks (73.91 kbps)
152	HDCP	HDMI-R10	+00:49:36.879371 R RxStatus (73.80 kbps)
153	HDCP	HDMI-R10	+00:49:36.879698 < 0000 (82.47 kbps)
154	HDCP	HDMI-R10	+00:49:37.080563 R RxStatus (73.69 kbps)
155	HDCP	HDMI-R10	+00:49:37.080727 < 0000 (82.47 kbps)
156	HDCP	HDMI-R10	+00:49:37.281592 R RxStatus (73.80 kbps)

EDID Details:

- Type: EDID
- Start Time: +00:49:32.400217
- Duration: 14.090 msec
- Maximum I2C Rate: 82.61 kbps
- Read 128 bytes.

```
* START *
0000 A1 02 03 4D F0 52 10 05 | . . . M . R . .
0008 20 22 04 03 02 07 06 5D | | . . . . . ]
0010 5E 5F 60 61 62 64 65 66 | ^ _ a b d e f
0018 23 0F 7F 07 78 03 0C 00 | # - . x . . .
0020 10 00 F8 3C 2F C8 8A 01 | . . . < / . . .
0028 02 03 04 81 41 00 16 06 | . . . A . . .
0030 08 00 56 58 00 67 D8 5D | . . . V X . g . ]
0038 C4 01 78 88 07 E2 00 4B | . . . x . . . K
0040 83 7F 00 00 E1 0F E3 06 | | . . . . .
0048 0F 01 E3 05 FF 00 01 1D | | . . . . .
0050 80 18 71 1C 16 20 58 2C | . . . q . . . X ,
0058 25 00 BA 88 21 00 00 9E | | % . . . ! . .
0060 66 21 56 AA 51 00 1E 30 | | f | V . Q . . . 0
0068 46 8F 33 00 BA 88 21 00 | | F . 3 . . . ! .
0070 00 1E 00 00 00 00 00 00 | | . . . . .
0078 00 00 00 00 00 00 00 00 | | . . . . .
0080 88- |
* STOP *
```

Aux Channel Analyzer (ACA) – HDCP Repeater Authentication

◆ HDMI Aux Channel Analyzer (ACA) for DDC monitoring:

- ◆ Enables monitoring and analysis of the HDMI connection sequence.
- ◆ Verify EDID exchange, HDCP authentication transactions.
- ◆ Supports search and filtering functions.
- ◆ Assigns precise timestamps for each transaction; provides user controls to associate events.
- ◆ Enables export of transaction logs to share with colleagues.

The screenshot displays the ACA Data Viewer interface with a list of events and a detailed view of a selected event. The event list shows various HDCP transactions between DPFP and HDCP components. The selected event is 'RepeaterAuth_Send_ReceiverID_List' at timestamp 00:14:51.762106. The detailed view on the right shows the register information for this event, including the register name 'RepeaterAuth_Send_ReceiverID_List', the message ID '12', and the receiver ID list 'ID-00: 570CEBA925'. Below the register information, there is a hex dump of the message data.

```
ACA Data Viewer
Open Close Export Options Filter Find
[ACMT_PT_Rpt_1_Pass] Events: 73
0 DPFP DP-T60 +00:14:19.537922 RFD Falling Edge
1 HDCP HDMI-R30 +00:14:50.714037 R HDCP2Version (73.91 kbps)
2 HDCP HDMI-R30 +00:14:50.714365 < 04 (82.47 kbps)
3 HDCP HDMI-R30 +00:14:50.719936 R RxStatus (73.80 kbps)
4 HDCP HDMI-R30 +00:14:50.720263 < 0000 (82.47 kbps)
5 HDCP HDMI-R30 +00:14:50.727308 W AKM_Init (73.91 kbps)
6 HDCP HDMI-R30 +00:14:50.783013 R RxStatus (73.80 kbps)
7 HDCP HDMI-R30 +00:14:50.783341 < 1602 (82.47 kbps)
8 HDCP HDMI-R30 +00:14:50.784160 R Read_Message (73.91 kbps)
9 HDCP HDMI-R30 +00:14:50.784488 < AKM_Send_Cert (82.61 kbps)
10 HDCP HDMI-R30 +00:14:51.030080 W AKM_No_Stored_km (74.02 kbps)
11 HDCP HDMI-R30 +00:14:51.246837 R RxStatus (73.91 kbps)
12 HDCP HDMI-R30 +00:14:51.247165 < 0000 (82.47 kbps)
13 HDCP HDMI-R30 +00:14:51.448029 R RxStatus (73.91 kbps)
14 HDCP HDMI-R30 +00:14:51.448357 < 2100 (82.47 kbps)
15 HDCP HDMI-R30 +00:14:51.449176 R Read_Message (73.91 kbps)
16 HDCP HDMI-R30 +00:14:51.449340 < AKM_Send_H_prime (82.47 kbps)
17 HDCP HDMI-R30 +00:14:51.503734 R RxStatus (73.80 kbps)
18 HDCP HDMI-R30 +00:14:51.504062 < 1100 (82.47 kbps)
19 HDCP HDMI-R30 +00:14:51.504881 R Read_Message (73.80 kbps)
20 HDCP HDMI-R30 +00:14:51.505045 < AKM_Send_Pairing_Info (82.47 kbps)
21 HDCP HDMI-R30 +00:14:51.518643 W LC_Init (73.91 kbps)
22 HDCP HDMI-R30 +00:14:51.540598 R RxStatus (73.80 kbps)
23 HDCP HDMI-R30 +00:14:51.540761 < 2100 (82.47 kbps)
24 HDCP HDMI-R30 +00:14:51.541581 R Read_Message (73.91 kbps)
25 HDCP HDMI-R30 +00:14:51.541908 < LC_Send_L_prime (82.47 kbps)
26 HDCP HDMI-R30 +00:14:51.553705 W SKM_Send_Eks (73.91 kbps)
27 HDCP HDMI-R30 +00:14:51.760795 R RxStatus (73.80 kbps)
28 HDCP HDMI-R30 +00:14:51.761123 < 1B04 (82.47 kbps)
29 HDCP HDMI-R30 +00:14:51.761942 R Read_Message (73.80 kbps)
30 HDCP HDMI-R30 +00:14:51.762106 < RepeaterAuth_Send_ReceiverID_List (82.47 kbps)
31 HDCP HDMI-R30 +00:14:51.769642 W RepeaterAuth_Send_Ack (73.91 kbps)
32 HDCP HDMI-R30 +00:14:51.776851 W RepeaterAuth_Stream_Manage (73.91 kbps)
33 HDCP HDMI-R30 +00:14:51.833211 R RxStatus (73.80 kbps)
34 HDCP HDMI-R30 +00:14:51.833375 < 2100 (82.47 kbps)
35 HDCP HDMI-R30 +00:14:51.834194 R Read_Message (73.91 kbps)
36 HDCP HDMI-R30 +00:14:51.834522 < RepeaterAuth_Stream_Ready (82.47 kbps)

Type: HDCP
Start Time: +00:14:51.762106
Duration: 3.113 msec
Maximum I2C Rate: 82.47 kbps
Read, 27 bytes
Register: 80h
Name: Read_Message
Message: RepeaterAuth_Send_ReceiverID_List (27 bytes)
MsgInfo: 12
RxInfo:
Bit Name Value Description
-----
0 HDCP1_DEVICE_DOWNSTREAM F(1)
1 HDCP2_LEGACY_DEVICE_DOWNSTREAM N(0)
2 MAX_CASCADE_EXCEEDED N(0)
3 MAX_DEVS_EXCEEDED N(0)
8-4 DEVICE_COUNT 1
11-9 DEPTH 1
15-12 Rsvd 0
seq_num_V: 0 (0000000h)
V [255..128]: 02 F3 D5 D6 A0 1E 87 04 DC 51 26 80 CD 3C A0
Receiver ID List:
ID-00: 570CEBA925

* START *
0000 75 0C 02 11 00 00 00 02 | u . . . . .
0008 F3 D5 D6 A0 1E 87 04 DC | | . . . . .
0010 51 26 80 CD 3C A0 BE 57 | Q & . . . . W
0018 0C EB A9 25- | . . . %
* STOP *
```

Aux Channel Analyzer (ACA) – Filtering

◆ HDMI Aux Channel Analyzer (ACA) Export:

- ◆ Filter the transaction list by interface, by type of transaction or by text strings.
- ◆ Search for specific transactions by text in the label text in the details of the message.

The screenshot shows the ACA Data Viewer interface with a list of transactions and an ACA Filter dialog box. The transaction list has columns for Open, Close, Export, Options, Filter, and Find. The ACA Filter dialog box has tabs for Open, Save, Clear, Add, and Remove. It contains a search bar with the text 'Where Src=HDMI-R60 AND Type=(EDID|SCDC|SCDC_...'. Below the search bar are columns for Source, Type, Label, and Detail. The 'Text contains:' field is checked, and the 'Regular Expression Syntax' field is unchecked. A yellow arrow points to the 'R Status' text in the Label field of the dialog box.

Open	Close	Export	Options	Filter	Find
0	SCDC	HDMI-R60	+00:35:51.358896	R Status_Flags_0	(48.86 kbps)
1	SCDC	HDMI-R60	+00:35:51.361681	R Status_Flags_0	(48.86 kbps)
2	SCDC	HDMI-R60	+00:35:51.364466	R Status_Flags_0	(48.86 kbps)
3	SCDC	HDMI-R60	+00:35:51.367252	R Status_Flags_0	(48.86 kbps)
4	SCDC	HDMI-R60	+00:35:51.370201	R Status_Flags_0	(48.86 kbps)
5	SCDC	HDMI-R60	+00:35:51.372986	R Status_Flags_0	(48.86 kbps)
6	SCDC	HDMI-R60	+00:35:51.375771	R Status_Flags_0	(48.86 kbps)
7	SCDC	HDMI-R60	+00:35:51.378556	R Status_Flags_0	(48.86 kbps)
8	SCDC	HDMI-R60	+00:35:51.381342	R Status_Flags_0	(48.86 kbps)
9	SCDC	HDMI-R60	+00:35:51.388223	R Status_Flags_0	(48.86 kbps)
10	SCDC	HDMI-R60	+00:35:51.391172	R Status_Flags_0	(48.86 kbps)
11	SCDC	HDMI-R60	+00:35:51.393957	R Status_Flags_0	(48.86 kbps)
12	SCDC	HDMI-R60	+00:35:51.396742	R Status_Flags_0	(48.86 kbps)
13	SCDC	HDMI-R60	+00:35:51.399528	R Status_Flags_0	(48.86 kbps)
14	SCDC	HDMI-R60	+00:35:51.402477	R Status_Flags_0	(48.86 kbps)
15	SCDC	HDMI-R60	+00:35:51.405262	R Status_Flags_0	(48.86 kbps)
16	SCDC	HDMI-R60	+00:35:51.408047	R Status_Flags_0	(48.86 kbps)
17	SCDC	HDMI-R60	+00:35:51.410832	R Status_Flags_0	(48.86 kbps)
18	SCDC	HDMI-R60	+00:35:51.413618	R Status_Flags_0	(48.86 kbps)
19	SCDC	HDMI-R60	+00:35:51.416403	R Status_Flags_0	(48.86 kbps)
20	SCDC	HDMI-R60	+00:35:51.419352	R Status_Flags_0	(48.86 kbps)
21	SCDC	HDMI-R60	+00:35:51.422137	R Status_Flags_0	(48.86 kbps)
22	SCDC	HDMI-R60	+00:35:51.424922	R Status_Flags_0	(48.86 kbps)
23	SCDC	HDMI-R60	+00:35:51.427708	R Status_Flags_0	(48.86 kbps)
24	SCDC	HDMI-R60	+00:35:51.430493	R Status_Flags_0	(48.86 kbps)
25	SCDC	HDMI-R60	+00:35:51.433442	R Status_Flags_0	(48.86 kbps)
26	SCDC	HDMI-R60	+00:35:51.436227	R Status_Flags_0	(48.86 kbps)
27	SCDC	HDMI-R60	+00:35:51.439668	R Status_Flags_0	(48.86 kbps)
28	SCDC	HDMI-R60	+00:35:51.442453	R Status_Flags_0	(48.86 kbps)
29	SCDC	HDMI-R60	+00:35:51.445402	R Status_Flags_0	(48.86 kbps)
30	SCDC	HDMI-R60	+00:35:51.448187	R Status_Flags_0	(48.86 kbps)
31	SCDC	HDMI-R60	+00:35:51.450973	R Status_Flags_0	(48.86 kbps)
32	SCDC	HDMI-R60	+00:35:51.453758	R Status_Flags_0	(48.86 kbps)
33	SCDC	HDMI-R60	+00:35:51.456543	R Status_Flags_0	(48.86 kbps)
34	SCDC	HDMI-R60	+00:35:51.459328	R Status_Flags_0	(48.86 kbps)

Aux Channel Analyzer (ACA) – Filtering

◆ HDMI Aux Channel Analyzer (ACA) Export:

- ◆ Filter the transaction list by interface, by type of transaction or by text strings.
- ◆ Search for specific transactions by text in the label text in the details of the message.

The screenshot shows the ACA Data Viewer interface. The main window displays a list of transactions with columns for time, interface, type, and data. A yellow arrow points to a transaction at time +00:35:51.35881 with the label '< 01 (48.86 kbps)'. To the right, a detailed view of this transaction is shown, including fields for Type (SCDC), Start Time, Duration, and Maximum I2C Rate. Below the details is an 'ACA Filter' dialog box with a search field containing 'Where Type=(EDID|SCDC|SCDC_UP|HDCP|HDMI-HPD)'. The dialog also has tabs for Source, Type, Label, and Detail, and a list of filterable items including Other, HDMI, eARC, MHL, DP, USB-C-PD, and USB4-DP. A yellow arrow points from the transaction list to the filter dialog.

Aux Channel Analyzer (ACA) – Searching

◆ HDMI Aux Channel Analyzer (ACA) Export:

- ◆ Filter the transaction list by interface, by type of transaction or by text strings.
- ◆ Search for specific transactions by text in the label text in the details of the message.

The screenshot displays the ACA Data Viewer application. The main window shows a list of transactions with columns for time, type, source, and data. Transaction 12 is highlighted. A yellow arrow points to the 'R Status_Flags_0' entry in the list. Another yellow arrow points to the 'Status_Flags_0' field in the details pane. A third yellow arrow points to the search filter 'Where Src=HDMI-R60 AND Type=(EDID|SCDC|SCDC_UP|HDCP) AND ...' in the search pane.

Time	Type	Source	Label
0	SCDC	HDMI-R60	+00:35:51.354636 R Update_0 (48.86 kbps)
1	SCDC	HDMI-R60	+00:35:51.355128 < 00 (48.86 kbps)
2	SCDC	HDMI-R60	+00:35:51.355455 W Update_0_00 (48.86 kbps)
3	SCDC	HDMI-R60	+00:35:51.356111 R Update_0 (48.86 kbps)
4	SCDC	HDMI-R60	+00:35:51.356438 < 00 (48.86 kbps)
5	SCDC	HDMI-R60	+00:35:51.356930 W Update_0_00 (48.86 kbps)
6	SCDC	HDMI-R60	+00:35:51.357421 R Sink Version (48.86 kbps)
7	SCDC	HDMI-R60	+00:35:51.357913 < 01 (48.86 kbps)
8	SCDC	HDMI-R60	+00:35:51.358241 W Source Version 01 (48.86 kbps)
9	SCDC	HDMI-R60	+00:35:51.358896 R Status_Flags_0 (48.86 kbps)
10	SCDC	HDMI-R60	+00:35:51.359224 < 01 (48.86 kbps)
11	SCDC	HDMI-R60	+00:35:51.361668 R Status_Flags_0 (48.86 kbps)
12	SCDC	HDMI-R60	+00:35:51.364446 < 01 (48.86 kbps)
13	SCDC	HDMI-R60	+00:35:51.364446 R Status_Flags_0 (48.86 kbps)
14	SCDC	HDMI-R60	+00:35:51.364958 < 01 (48.86 kbps)
15	SCDC	HDMI-R60	+00:35:51.367252 R Status_Flags_0 (48.86 kbps)
16	SCDC	HDMI-R60	+00:35:51.367743 < 01 (48.86 kbps)
17	SCDC	HDMI-R60	+00:35:51.370201 R Status_Flags_0 (48.86 kbps)
18	SCDC	HDMI-R60	+00:35:51.370528 < 01 (48.86 kbps)
19	SCDC	HDMI-R60	+00:35:51.372986 R Status_Flags_0 (48.86 kbps)
20	SCDC	HDMI-R60	+00:35:51.373314 < 01 (48.86 kbps)
21	SCDC	HDMI-R60	+00:35:51.375771 R Status_Flags_0 (48.86 kbps)
22	SCDC	HDMI-R60	+00:35:51.376099 < 01 (48.86 kbps)
23	SCDC	HDMI-R60	+00:35:51.378556 R Status_Flags_0 (48.86 kbps)
24	SCDC	HDMI-R60	+00:35:51.378884 < 01 (48.86 kbps)
25	SCDC	HDMI-R60	+00:35:51.381342 R Status_Flags_0 (48.86 kbps)
26	SCDC	HDMI-R60	+00:35:51.381669 < 01 (48.86 kbps)
27	SCDC	HDMI-R60	+00:35:51.388223 R Status_Flags_0 (48.86 kbps)
28	SCDC	HDMI-R60	+00:35:51.388714 < 01 (48.86 kbps)
29	SCDC	HDMI-R60	+00:35:51.391172 R Status_Flags_0 (48.86 kbps)
30	SCDC	HDMI-R60	+00:35:51.391500 < 01 (48.86 kbps)
31	SCDC	HDMI-R60	+00:35:51.393957 R Status_Flags_0 (48.86 kbps)
32	SCDC	HDMI-R60	+00:35:51.394285 < 01 (48.86 kbps)
33	SCDC	HDMI-R60	+00:35:51.396742 R Status_Flags_0 (48.86 kbps)
34	SCDC	HDMI-R60	+00:35:51.397234 < 01 (48.86 kbps)

Transaction 12 details:

Type: SCDC
Start Time: +00:35:51.362173
Duration: 164 to 328 us
Maximum I2C Rate: 48.86 kbps
Read, 1 byte
40h: Status_Flags_0

Bit	Name	Value	Description
0	Ch0_Detected	Y(1)	
1	Ch0_Locked	N(0)	
2	Ch1_Locked	N(0)	
3	Ch2_Ln2_Locked	N(0)	
4	Lane3_Locked	N(0)	

ACA Find

Open Save Clear Add Remove

Where Src=HDMI-R60 AND Type=(EDID|SCDC|SCDC_UP|HDCP) AND ...

Source	Type	Label	Detail
--------	------	-------	--------

Text contains: ON

NOT

Locked

Regular Expression Syntax ON

Found Event #13

PREVIOUS NEXT

CLOSE

Aux Channel Analyzer (ACA) – Export Transaction Data

◆ HDMI Aux Channel Analyzer (ACA) Export:

- ◆ Save ACA log as an HTML file.
- ◆ Export capture data to disseminate to colleagues, other subject matter experts or Teledyne Customer Support.
- ◆ Exported capture does not require M41h instrument; only requires ATP Manager.
- ◆ Transfer to PC to save and recall later for analysis.

The screenshot shows the ACA Data Viewer interface. The main window displays a list of events with columns for Operation, Source, Sink, Time, and Data. An arrow points to the 'Export' button in the top menu. Another arrow points to the 'Export as...' dialog box, which is open and shows the 'Events' section with 'All' selected and 'Range' set to '1 - 866'. The 'File Format' section has 'Text' and 'HTML' buttons, with 'HTML' selected. The 'OK' and 'CANCEL' buttons are at the bottom of the dialog.

Oper	Source	Sink	Time	Data
0	SCDC	HDMI-R60	+00:35:51.354636	R Update_0 (48.86 kbps)
1	SCDC	HDMI-R60	+00:35:51.355128	< 00 (48.86 kbps)
2	SCDC	HDMI-R60	+00:35:51.355455	W Update_0 00 (48.86 kbps)
3	SCDC	HDMI-R60	+00:35:51.356111	R Update_0 (48.86 kbps)
4	SCDC	HDMI-R60	+00:35:51.356438	< 00 (48.86 kbps)
5	SCDC	HDMI-R60	+00:35:51.356930	W Update_0 00 (48.86 kbps)
6	SCDC	HDMI-R60	+00:35:51.357421	R Sink Version (48.86 kbps)
7	SCDC	HDMI-R60	+00:35:51.357913	< 01 (48.86 kbps)
8	SCDC	HDMI-R60	+00:35:51.358241	W Source Version 01 (48.86 kbps)
9	SCDC	HDMI-R60	+00:35:51.358896	R Status_Flags_0 (48.86 kbps)
10	SCDC	HDMI-R60	+00:35:51.359224	< 01 (48.86 kbps)
11	SCDC	HDMI-R60	+00:35:51.361681	R Status_Flags_0 (48.86 kbps)
12	SCDC	HDMI-R60	+00:35:51.362173	< 01 (48.86 kbps)
13	SCDC	HDMI-R60	+00:35:51.364466	R Status_Flags_0 (48.86 kbps)
14	SCDC	HDMI-R60	+00:35:51.364958	< 01 (48.86 kbps)
15	SCDC	HDMI-R60	+00:35:51.367252	R Status_Flags_0 (48.86 kbps)
16	SCDC	HDMI-R60	+00:35:51.367743	< 01 (48.86 kbps)
17	SCDC	HDMI-R60	+00:35:51.370201	R Status_Flags_0 (48.86 kbps)
18	SCDC	HDMI-R60	+00:35:51.370528	< 01 (48.86 kbps)
19	SCDC	HDMI-R60	+00:35:51.372986	R Status_Flags_0 (48.86 kbps)
20	SCDC	HDMI-R60	+00:35:51.373314	< 01 (48.86 kbps)
21	SCDC	HDMI-R60	+00:35:51.375771	R Status_Flags_0 (48.86 kbps)
22	SCDC	HDMI-R60	+00:35:51.376099	< 01 (48.86 kbps)
23	SCDC	HDMI-R60	+00:35:51.378556	R Status_Flags_0 (48.86 kbps)
24	SCDC	HDMI-R60	+00:35:51.378884	< 01 (48.86 kbps)
25	SCDC	HDMI-R60	+00:35:51.381342	R Status_Flags_0 (48.86 kbps)
26	SCDC	HDMI-R60	+00:35:51.381669	< 01 (48.86 kbps)
27	SCDC	HDMI-R60	+00:35:51.388223	R Status_Flags_0 (48.86 kbps)
28	SCDC	HDMI-R60	+00:35:51.388714	< 01 (48.86 kbps)
29	SCDC	HDMI-R60	+00:35:51.391172	R Status_Flags_0 (48.86 kbps)
30	SCDC	HDMI-R60	+00:35:51.391500	< 01 (48.86 kbps)
31	SCDC	HDMI-R60	+00:35:51.393957	R Status_Flags_0 (48.86 kbps)
32	SCDC	HDMI-R60	+00:35:51.394285	< 01 (48.86 kbps)
33	SCDC	HDMI-R60	+00:35:51.396742	R Status_Flags_0 (48.86 kbps)
34	SCDC	HDMI-R60	+00:35:51.397234	< 01 (48.86 kbps)

Aux Channel Analyzer (ACA) – Export Transaction Data

◆ HDMI Aux Channel Analyzer (ACA) Export:

- ◆ Save ACA log as an HTML file.
- ◆ Export capture data to disseminate to colleagues, other subject matter experts or Teledyne Customer Support.
- ◆ Exported capture does not require M41h instrument; only requires ATP Manager.
- ◆ Transfer to PC to save and recall later for analysis.

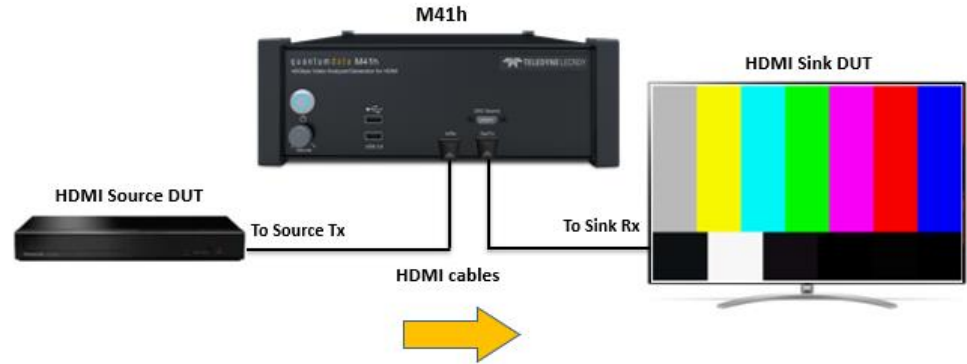
The screenshot shows the ATP Manager software interface. On the left, the 'ACA Trace' menu is open, and the 'Export' option is highlighted with a yellow arrow. The main window displays a list of capture files with columns for Name and Date / Time. The file 'ACMT_PT_Rpt_1_Pass' is selected, and a yellow arrow points to it. On the right, the 'quantumdata' application is visible, showing a control panel with buttons for Generator, Receiver, ACA Remote Control, and HEAC.

Name	Date / Time
DP_LT_4K_81_4L_HDCP_1	2020/05/30 16:52:45
DP_LT_4K_81_4L_2	2020/05/09 11:26:34
DP_LT_4K_81_4L	2020/05/09 11:26:34
DP_LT_4K_4L_54LR	2020/05/09 11:26:34
DP_LT_13_1080_4L_54LR_1	2020/05/09 11:26:34
DP_LT_1080p_4L_54LR_2_HDCP	2020/06/01 19:34:27
DP_LT_1080p_4L_54LR	2020/05/09 11:26:34
DP_LT_1080p_2L_27LR	2020/05/09 11:26:34
DP_DSC_FEC_NV	2020/05/09 11:26:34
DP_DSC_FEC_MV	2020/05/09 11:26:34
DP_DSC_FEC_LT_1	2020/05/09 11:26:34
DP_DSC_2	2020/05/09 11:26:34
DP_14_4K_HDCP_22	2020/05/09 11:26:33
DP_14_4K	2020/05/09 11:26:33
CDS_Read	2020/05/09 11:26:33
CC_TI	2020/05/09 11:26:33
ACMT_Sink_NoHDCP	2020/05/09 11:26:33
ACMT_Sink_EDID	2020/05/09 11:26:33
ACMT_Sink	2020/05/09 11:26:33
ACMT_Pass_Rpt_1_Pass2	2020/05/09 11:26:33
ACMT_Pass_Rpt_0_Pana_Pass	2020/05/09 11:26:33
ACMT_PassE_Rpt_1_Pana_Fail	2020/05/09 11:26:33
ACMT_PassE_Rpt_0_Pana_Pass	2020/05/09 11:26:33
ACMT_PassE_Rpt_0_LG_Pass	2020/05/09 11:26:33
ACMT_PT_Rpt_1_Pass	2020/05/09 11:26:33
ACMT_PT_Rpt_0_Pass2	2020/05/09 11:26:33
ACMT_PT_Rpt_0_Pass	2020/05/09 11:26:33
ACMT_PT_Rpt_0_2	2020/05/09 11:26:33
ACMT_PT_Rpt_0	2020/05/09 11:26:33
ACMT_HDCP_fallback	2020/05/09 11:26:33
ACMT_HDCP_1B_10_2	2020/05/09 11:26:33
ACMT_HDCP_1B_07_2	2020/05/09 11:26:33
ACMT_HDCP_1B_06_2_Fail	2020/05/09 11:26:33
ACMT_HDCP_1B_01_Pass	2020/05/09 11:26:33
ACMT_HDCP_1A_06_1	2020/05/09 11:26:33
ACMT_HDCP_1A_04_1	2020/05/09 11:26:33
ACMT_HDCP_1A_01_2	2020/05/09 11:26:33
AA_LaptopNV_USB_to_980_USB	2020/05/09 11:26:33
AA_LaptopMB_USB_to_980_USB_Err	2020/05/09 11:26:33
AA_LaptopMR_USB_to_980_USB	2020/05/09 11:26:33

HDMI DDC Passive Monitoring TMDS and FRL modes

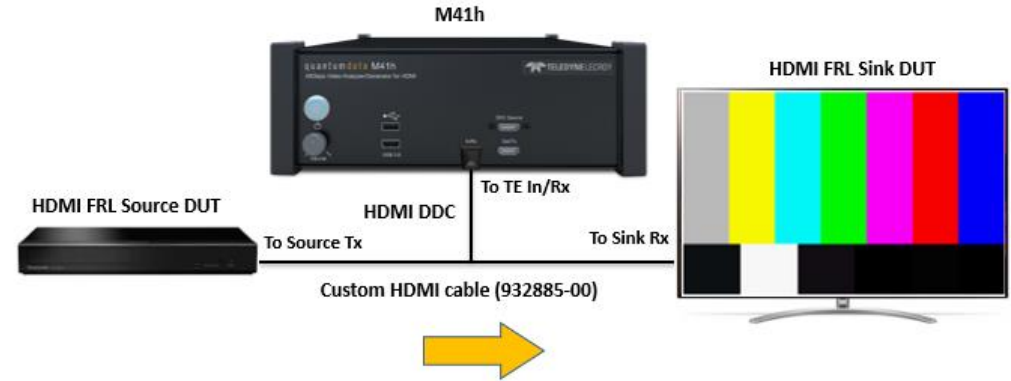
HDMI DDC Passive Monitoring – TMDS Mode

- ◆ Passive monitoring of DDC channel
 - ◆ You can monitor the DDC channel passively in the **TMDS** mode by connecting a source to the M41h Rx port and a sink to the M41h Tx port.
 - ◆ The ability to passively monitor the DDC channel in the TMDS mode is important for EDID and HDCP authentication interoperability.



HDMI DDC Passive Monitoring – FRL Mode

- ◆ Passive monitoring of DDC channel
 - ◆ You can optionally monitor the DDC channel passively in the **FRL** mode using a custom cable (setup right).
 - ◆ The DDC passive monitoring enables you to diagnose interoperability problems between a source and a display.
 - ◆ The ability to passively monitor the DDC channel in the FRL mode with the custom cable is especially important for FRL link training, EDID and HDCP authentication interoperability.



HDMI 2.1 Source Testing Compliance Testing

HDMI Fixed Rate Link (FRL) Source Compliance Test

◆ HDMI 2.1 FRL source compliance Testing:

- ◆ Run FRL source compliance tests. Full list of tests supported (only partial list shown right).



The screenshot shows the 'FRL Source' application window. At the top, it displays 'Instrument: AL_M41d [10.30.196.30]' and 'Connect Cards'. Below this is a navigation bar with 'CDF Entry', 'Test Selection', and 'Test Options / Preview'. A toolbar contains 'Select All', 'Duration', 'Options', and a green 'EXECUTE TESTS' button. The main area is a table of tests, each with a dropdown arrow, a description, and a green checkmark in the rightmost column. The tests are grouped into categories: Protocol, Link Training, 8bpc Encoding, DC Encoding, 8bpc Timing, and DC Timing.

Test ID	Description	Status
Protocol		
> HFR1-11:	Source FRL Protocol - Legal Codes	✓
> HFR1-19:	Source FRL Packets - FRL Map Characters	✓
> HFR1-20:	Source FRL Packets - FRL Control Periods	✓
> HFR1-21:	Source FRL Packets - Active Video FRL Packets (Uncompressed)	✓
> HFR1-23:	Source FRL Protocol - Data Flow Metering Variations	✓
Link Training		
> HFR1-10:	Source FRL Protocol - FRL Link Training Patterns	✓
> HFR1-12:	Source FRL Protocol - Successful FRL Link Training	✓
> HFR1-13:	Source FRL Protocol - FRL Link Training - Link Rate Change	✓
> HFR1-17:	Source FRL Protocol - FRL Link Training - Future Rate Support	✓
8bpc Encoding		
> HFR1-29:	Source Pixel Encoding (FRL Mode) - RGB	✓
> HFR1-30:	Source Pixel Encoding (FRL Mode) - YCBCR 4:2:2/4:4:4	✓
> HFR1-31:	Source Pixel Encoding (FRL Mode) - YCBCR 4:2:0	✓
DC Encoding		
> HFR1-27:	Source Pixel Encoding (FRL Mode) - Non-YCBCR 4:2:0 Deep Color	✓
> HFR1-32:	Source Pixel Encoding (FRL Mode) - YCBCR 4:2:0 Deep Color	✓
8bpc Timing		
> HFR1-14:	Source Video Timing (FRL Mode) - Sub-2160p 24-bit Color Depth	✓
> HFR1-24:	Source Video Timing (FRL Mode) - 2160p 24-bit Color Depth	✓
> HFR1-33:	Source Video Timing (FRL Mode) - YCBCR 4:2:0	✓
> HFR1-50:	Source Video Timing (FRL Mode) - 4320p 24-bit Color Depth	✓
DC Timing		
> HFR1-15:	Source Video Timing (FRL Mode) - Sub-2160p Deep Color	✓
> HFR1-25:	Source Video Timing (FRL Mode) - 2160p Deep Color	✓
> HFR1-34:	Source Video Timing (FRL Mode) - YCBCR 4:2:0 Deep Color	✓

HDMI Fixed Rate Link (FRL) Source Compliance Test

- ◆ HDMI 2.1 FRL source compliance Testing:
 - ◆ Run FRL source compliance tests. Full list of tests supported.
 - ◆ Provides detailed Test Results with Pass/Fail and details for each subtest.
 - ◆ Enables compliance self-testing and/or pre-testing of FRL devices.
 - ◆ Enables export of compliance test results to share with colleagues.

Test Name / Details	Status
HFR1-11: Source FRL Protocol - Legal Codes	Pass
Iter 01: FRL 3 Lane Mode	Pass
Trained at: (2) 6 Gbps @ 3 Lanes	
01: Test that the FRL characters count and SSB/SR characters count is valid.	Pass
02: SR header occurs only after 32 super blocks and at SB count '0'.	Pass
03: Illegal codes or other related errors associated with this test case.	Pass
04: SSB/SR header occurs only prior to Character block '0'.	Pass
Iter 02: FRL 4 Lane Mode	Pass
HFR1-19: Source FRL Packets - FRL Map Characters	Pass
Iter 01: Lowest FRL Rate in 3 Lane mode	Pass
Iter 02: Lowest FRL Rate in 4 Lane mode	Pass
Trained at: (3) 6 Gbps @ 4 Lanes	
01: Test that the FRL MAP Type is valid.	Pass
02: Test that Video Blanking/Video Data Characters Length is greater than 1	Pass
03: Test That the sum of all MAP Length fields in a Super Block is 2008.	Pass
HFR1-20: Source FRL Packets - FRL Control Periods	Pass
HFR1-21: Source FRL Packets - Active Video FRL Packets (Uncompressed)	Fail
Iter 01: Lowest FRL Rate in 3 Lane mode	Fail
Trained at: (1) 3 Gbps @ 3 Lanes	
01: Test that the Source only outputs legal Active Video FRL Packets.	Fail
02: Test that the video data characters are not separated by video blanking	Pass
03: Test that the last second byte of the 16-bit value of active video data	Pass
Iter 02: Lowest FRL Rate in 4 Lane mode	Fail
HFR1-23: Source FRL Protocol - Data Flow Metering Variations	Pass
HFR1-12: Source FRL Protocol - Successful FRL Link Training	Pass
HFR1-13: Source FRL Protocol - FRL Link Training - Link Rate Change	Pass
HFR1-17: Source FRL Protocol - FRL Link Training - Future Rate Support	Pass

HDMI FRL Display Stream Compression Source Compliance Test

- ◆ HDMI 2.1 FRL source compliance Testing:
 - ◆ Run FRL DSC source compliance tests. Full list of tests supported.
 - ◆ Provides detailed Test Results with Pass/Fail and details for each subtest.
 - ◆ Enables compliance self-testing and/or pre-testing of FRL DSC devices.
 - ◆ Enables export of compliance test results to share with colleagues.

Compliance Test Results Viewer

FRL Source Compliance Test Results

HTML Report Instrument: MyM41d[10.30.196.25]

Results Name: hfr1-83-1 Manufacturer: acme

Date Tested: January 14, 2021 3:04 PM Model Name: xyz

Overall Status: Pass Port Tested: 1

Test Name	Status	Details
HFR1-83: Source Video Timing (DSC) - 4320p 10 bpc/12 bpc RGB Primary Compressed Formats	PASS	
Iter 01: (196) 7680x4320p @ 30 Hz, RGB, 10 bpc, MAX FRL Rate (4/12G)	PASS	5 f 1
Trained at: (6) 12 Gbps @ 4 Lanes		
Visual verification: The image was transmitted correctly.		
01: Verify that the Source transmits CVTEM packets	PASS	
02: Verify that the PPS fields meet the requirements in HDMI 2.1 Table 7-25	PASS	
03: Verify that the PPS field bits_per_component = 10	PASS	
04: Verify that the bits_per_pixel value in the PPS matches the primary Compressed Format	PASS	
05: Verify that the values of Hfront, Hsync, Hback, and Hactive_bytes equal the correct value for the selected Video Format	PASS	
06: Verify that the pixel repetition flag in the AVI InfoFrame Packet is not set	PASS	
07: Verify that the pixel frequency is within +/- 0.5% of the expected rate	PASS	
08: Verify that every GCP packet has the Color Depth (CD), Pixel Packing Phase (PP), and Default_Phase fields set to zero	PASS	
09: Verify that all of the Video Data Periods have the correct length and that all VSYNC positions and lengths are accurate	PASS	
10: Verify that the compressed video can be successfully decoded using the DSC C Model	PASS	
11: Verify that received test pattern matches the definition in Appendix E (if supported by the DUT)	PASS	
Iter 02: (196) 7680x4320p @ 30 Hz, RGB, 10 bpc, MIN FRL Rate (3/6G), HF-SCDB	PASS	5 f 1
Trained at: (2) 6 Gbps @ 3 Lanes		
Visual verification: The image was transmitted correctly.		
01: Verify that the Source transmits CVTEM packets	PASS	
02: Verify that the PPS fields meet the requirements in HDMI 2.1 Table 7-25	PASS	
03: Verify that the PPS field bits_per_component = 10	PASS	
04: Verify that the bits_per_pixel value in the PPS matches the primary Compressed Format	PASS	
05: Verify that the values of Hfront, Hsync, Hback, and Hactive_bytes equal the correct value for the selected Video Format	PASS	
06: Verify that the pixel repetition flag in the AVI InfoFrame Packet is not set	PASS	
07: Verify that the pixel frequency is within +/- 0.5% of the expected rate	PASS	
08: Verify that every GCP packet has the Color Depth (CD), Pixel Packing Phase (PP), and Default_Phase fields set to zero	PASS	

Open Capture | HFR1-83: Source Video Timing (DSC) - 4320p 10 bpc/12 bpc RGB Primary Compressed Formats

HDMI TMDS Source Compliance Testing

◆ HDMI TMDS compliance Testing:

- ◆ Run TMDS source compliance tests. Full list of tests supported (only partial list shown right).
- ◆ Provides detailed Test Results with Pass/Fail and details for each subtest.
- ◆ Enables compliance self-testing and/or pre-testing of HDMI TMDS devices.
- ◆ Enables export of compliance test results to share with colleagues.

Test Selection	Test Options / Preview
Select All	EXECUTE TESTS
TMDS Protocol	
> HF1-10: TMDS Protocol - 6G - TMDS Bit Clock Ratio	✓
> HF1-11: Source TMDS Protocol - 6G Legal Codes	✓
> HF1-12: TMDS Protocol - 6G - Basic Protocol and Scrambling	✓
> HF1-13: TMDS Protocol - Scrambling <= 3.4Gbps	✓
> HF1-21: TMDS Protocol - 6G - Legal Codes - other Video Timings	✓
> HF1-22: TMDS Protocol - 6G - Basic Protocol and Scrambling - Other Video Timings	✓
Pixel Encoding	
> HF1-31: Pixel Encoding - YCBCR 4:2:0 - TMDS Pixel Encoding	✓
> HF1-32: Pixel Encoding - YCBCR 4:2:0 Deep Color - TMDS Pixel Encoding	✓
Video Timing	
HF1-14: Video Timing - 6G - 2160p 24-bit Color Depth	✗
> HF1-15: Video Timing - 6G - Deep Color	✓
> HF1-16: Video Timing - 6G - 2160p 3D	✓
> HF1-24: Video Timing - 6G - Other 24-bit Color Depth	✓
> HF1-25: Video Timing - 6G - Other Deep Color	✓
> HF1-26: Video Timing - 6G - Non-2160p 3D	✓
> HF1-33: Video Timing - YCBCR 4:2:0	✓
> HF1-34: Video Timing - YCBCR 4:2:0 Deep Color	✓
> HF1-35: Video Timing - 21:9 (64:27)	✓
> HF1-71: Video Timing - YCbCr 4:2:0 for 861G Video Formats	✓
> HF1-72: Video Timing - YCbCr 4:2:0 Deep Color for 861G Video Formats	✓
AVI-IF/GCP	
> HF1-18: AVI InfoFrame - 6G	✓
> HF1-28: AVI InfoFrame - 6G - Other Video Timings	✓
> HF1-51: AVI InfoFrame for Y420VDB and Y420C MDB	✓
> HF1-52: AVI InfoFrame and GCP - YCbCr 4:2:0 BT.2020	✓

HDMI TMDS Source Compliance Testing

- ◆ HDMI TMDS compliance Testing:
 - ◆ Run TMDS source compliance tests. Full list of tests supported.
 - ◆ Provides detailed Test Results with Pass/Fail and details for each subtest.
 - ◆ Enables compliance self-testing and/or pre-testing of HDMI TMDS devices.
 - ◆ Enables export of compliance test results to share with colleagues.

Test Name / Details	Status
HF1-10: TMDS Protocol - 6G - TMDS Bit Clock Ratio	Pass
Iter 01: Any supported format above 340Msc	Pass
Iter 02: 640x480p, 720x480p, or 720x576p	Pass
The output of command "sdc stat" are:	
• TMDS CLOCK RATIO: 1/10	
• SCRAMBLING : DISABLED	
• SCRAMBLER STATUS: OFF	
• CLOCK : DETECTED	
• READ REQUEST : DISABLED	
• CH0 : LOCKED	
• CH1 : LOCKED	
• CH2 : LOCKED	
01: Verify Source DUT writes 0 to the TMDS Bit Clock Ratio bit after it outputs 6	Pass
HF1-11: Source TMDS Protocol - 6G Legal Codes	Pass
Iter 01: 2160p Format with lowest TMDS Character Rate above 340Msc	Pass
HF1-12: TMDS Protocol - 6G - Basic Protocol and Scrambling	Pass
Iter 01: 2160p Format with lowest TMDS Character Rate above 340Msc	Pass
Measured TMDS rate: 594.0 Msc	
01: HF1-12 4.2 Check if scrambling Enable bit is set	Pass
02: HF1-12 4.3.1 Check if number of unscrambled control codes is not greater	Pass
03: HF1-12 4.3.2 Check if number of unscrambled control codes is not less tha	Pass
04: HF1-12 4.3.3 Check if only one unscrambled control period per field	Pass
05: HF1-12 4.5 Check if no ENC EN code (CTL0:3=1001) is included	Pass
06: HF1-12 4.6.1 Validate Data Island Preamble coding	Pass
07: HF1-12 4.6.2 Validate Usage of Data Island Preamble control code	Pass
08: HF1-12 4.6.3 Check Preamble Consistency	Pass
09: HF1-12 4.7 Validate legal Preamble	Pass
10: HF1-12 4.8.1.1 Validate TMDS channel 0 character in Data Island Leading Gua	Pass
11: HF1-12 4.8.1.2 Validate Data Island Leading Guard Band	Pass
12: HF1-12 4.8.2 Validate Data Island Coding	Pass

HDMI TMDS Gaming Source Compliance Test

◆ HDMI 2.1 TMDS Gaming sink compliance Testing:

- ◆ Run TMDS Gaming sink compliance tests:
 - ◆ Quick Frame Transport (QFT).
 - ◆ Variable Refresh Rate (VRR).
 - ◆ Quick Media Switching (QMS).
 - ◆ VRR with QFT.
 - ◆ ALLM – (Future)
- ◆ Provides detailed Test Results with Pass/Fail and details for each subtest.
- ◆ Enables compliance self-testing and/or pre-testing of TMDS Gaming-capable devices.
- ◆ Enables export of compliance test results to share w/ colleagues.

The screenshot shows the 'FRL Source' application window. At the top, it displays 'Instrument: MyM41h [10.30.196.32]' and 'Connect Cards'. Below this is a navigation bar with 'CDF Entry', 'Test Selection', and 'Test Options / Preview'. A toolbar includes 'Select All', 'Duration', 'Options', and a prominent 'EXECUTE TESTS' button. The main area is a table with a tree view under the heading 'Gaming'. The table lists several test categories and their results:

Test Category	Result	Status
◆ Gaming		
◆ HF1-56: Auto Low-Latency Mode for Sources		✓
• Iter 01: Source_Supports_ALLM = 'N': Automatic PASS(SKIP)	--	✓
◆ HF1-57: Quick Frame Transport for Sources		✓
• Iter 01: Source_Supports_FVA = 'N': Automatic PASS(SKIP)	--	✓
◆ HF1-58: Variable Refresh Rate for Sources		✓
• Iter 01: Source_Supports_VRR = 'N': Automatic PASS(SKIP)	--	✓
◆ HF1-59: Quick Media Switching for Sources		✓
• Iter 01: Source_Supports_QMS = 'N': Automatic PASS(SKIP)	--	✓
◆ HF1-60: VRR with QFT for Sources		✓
• Iter 01: Source_Supports_VRR = 'N': Automatic PASS(SKIP)	--	✓

A 'CLOSE' button is located at the bottom right of the window.

HDMI TMDS Gaming Source Compliance Test

- ◆ HDMI 2.1 TMDS Gaming sink compliance Testing:

- ◆ Run TMDS Gaming sink compliance tests:
 - ◆ Quick Frame Transport (QFT).
 - ◆ Variable Refresh Rate (VRR).
 - ◆ Quick Media Switching (QMS).
 - ◆ VRR with QFT.
 - ◆ ALLM – (Future)
- ◆ Provides detailed Test Results with Pass/Fail and details for each subtest.
- ◆ Enables compliance self-testing and/or pre-testing of TMDS Gaming-capable devices.
- ◆ Enables export of compliance test results to share w/ colleagues.

The screenshot shows the 'FRL Source Compliance Test (2.1b): "NK_Game_Matt"' application. The main window displays a 'Test List' table with columns for 'Category / Test Name', 'Status', and 'Test Name'. An orange arrow points to the 'Gaming' category. The test list includes several subtests, with 'HF1-56: Auto Low-Latency Mode for Sources' and 'HF1-57: Quick Frame Transport for Sources' highlighted in yellow. The 'HF1-56' subtest is currently 'In Progress', while 'HF1-57' is 'Incomplete'. Below the test list is a 'Test Log' window showing the progress of the current test, including messages like 'Capturing data...', 'Post Capture Processing', and 'Generating video content data...'. At the bottom of the application, there are buttons for 'Cancel the Compliance Test' and 'Pause Test Execution'.

Category / Test Name	Status
Gaming	✓
HF1-56: Auto Low-Latency Mode for Sources	In Progress
Iter 01: Verify HF-VSIF with non-ALLM EDID	Fail
Iter 02: Verify HF-VSIF with ALLM EDID	Pass
Iter 03: Verify Video	In Progress
HF1-57: Quick Frame Transport for Sources	Incomplete
Iter 01: 720p60 RGB 8 bpc, FF1: No VTEMs Transmitted	Not Tested
Iter 02: Timing #1: 1920x1080-60 FF2-4	Not Tested
Iter 03: Interlaced	User Skipped
Iter 04: Any Timing, FVA Factor=2	User Skipped
Iter 05: Any Timing, Highest Supported FVA Factor	User Skipped
HF1-58: Variable Refresh Rate for Sources	Incomplete
Iter 01: VRR48-60, VRR Disabled	Not Tested
Iter 02: 1080p60 RGB 8 bpc, VRR48-60	Not Tested
Iter 03: 1080p60 RGB 8 bpc, VRR48-60, Stressed	User Skipped
Iter 04: 1080p120 RGB 8 bpc, VRR48-60	User Skipped
Iter 05: 1080p120 RGB 8 bpc, VRR48-60, Stressed	User Skipped
Iter 06: 1080p120 RGB 8 bpc, VRR48-100	User Skipped
Iter 07: 1080p120 RGB 8 bpc, VRR48-100, Stressed	User Skipped
Iter 08: 1080p120 RGB 8 bpc, VRR48-110	User Skipped
Iter 09: 1080p120 RGB 8 bpc, VRR48-110, Stressed	User Skipped
Iter 10: 1080p120 RGB 8 bpc, VRR48-120	User Skipped
Iter 11: 1080p120 RGB 8 bpc, VRR48-120, Stressed	User Skipped

Line	Message
0103	Capturing data...
0104	Post Capture Processing
0105	Generating video content data...
0106	-- preprocess 0 frames
0107	-- preprocess 14 frames
0150	-- preprocess 440 frames
0151	Preparing verification images
0152	Generating a verification image.

HDMI TMDS Gaming Source Compliance Test

- ◆ HDMI 2.1 TMDS Gaming sink compliance Testing:

- ◆ Run TMDS Gaming sink compliance tests:
 - ◆ Quick Frame Transport (QFT).
 - ◆ Variable Refresh Rate (VRR).
 - ◆ Quick Media Switching (QMS).
 - ◆ VRR with QFT.
 - ◆ ALLM – (Future)
- ◆ Provides detailed Test Results with Pass/Fail and details for each subtest.
- ◆ Enables compliance self-testing and/or pre-testing of TMDS Gaming-capable devices.
- ◆ Enables export of compliance test results to share w/ colleagues.

PORT:486 Protocol Analyzer HDMI RX - RX
Update Cnt: 139 Type: FRL 6 Char Rate: 656.94 HDCP: NONE PasTh: 0 SCAN: Progressive
Active: 2380 x 4320 Total: 2496 x 4400 H-Sync: F:0 W:0 P: V-Sync: F:16 W:20 P:+
CTA VIC:199: 7680x4320p @ 60 Hz 16:9 7680 x 4320 Progressive 30 bpp, YCbCr-420, BT_2020-YCC Not Encrypted DSC

Video Timing: 2 / 47
L=N, Hfreq=31.5000 kHz, Vfreq=50.4000 Hz, TMDS Clock Freq=27.02700 MHz, Type=HDMI

H/V	Htotal	Hblank	Vtotal	Vblank	Hfront	Hsync	Hback	Vfront	Vsync	Vback
0	858	138	625	145	16	62	60	109	6	30
0	858	138	625	145	16	62	60	109	6	30
0	858	138	625	145	16	62	60	109	6	30

EMP: 89 (32) 145

Pause Clear Show Ref Set Ref

Extended Metadata Packet

First DSF: 0
Last DSF: 1
Sequence Index: 5
MD (133): 02 e4 1b 00 00 00 00
MD (140): 00 00 00 00 00 00 00
MD (147): 00 00 00 00 00 00 00
MD (154): 00 00 00 00 00 00 00

HB: 7f 40 05 d2
SP0: 02 e4 1b 00 00 00 00 49
SP1: 00 00 00 00 00 00 00
SP2: 00 00 00 00 00 00 00
SP3: 00 00 00 00 00 00 00
#

Compliance Testing – Export Compliance Test Results

◆ HDMI Aux Compliance Test Results Export:

- ◆ Save compliance test results and HTML file for easy and universal viewing through browser.

HTML Viewer

C:\Users\mkendall\Documents\Current_Work\M4_980_Data_New\A_DataSet4\flsrctt\results\AA_XLN_LT_MOI_11_19\Report_Cdf.htm

June 2, 2020 8:05 PM www.quantumdata.com

HDMI FRL Source Compliance Test Report

Results Name:	AA_XLN_LT_MOI_11_19	Manufacturer:	xilinx
Date Tested:	October 24, 2018 3:50 PM	Model Name:	hdmi2.1
Overall Status:	Pass	Port Tested:	1

Report Index / Summary

Test HFR1-11	Pass	Test HFR1-19	Pass	CDF
Equipment Info				

Capabilities Declaration Form (CDF)

General	
CDF_TEST_PERIOD	2000
QD_HP_LENGTH	
QD_LPCM_Modes	
FRL	
Source_Max_FRL_Rate	10 Gbps @ 4 Lanes
Source_Max_TxFE	0
Features	
Source_Supports_4K100A	YES
Source_Supports_4K100B	YES
Source_Supports_4K120A	YES
Source_Supports_4K120B	YES
Source_Supports_8K50A	YES
Source_Supports_8K50B	YES
Source_Supports_8K60A	YES
Source_Supports_8K60B	YES
DSC	
Source_DSC_Max_FRL_Rate	Not Supported

BACK FORWARD SAVE AS... CLOSE

Compliance Testing – Export Compliance Test Results

◆ HDMI Aux Compliance Test Results Export:

- ◆ Save compliance test results and HTML file for easy and universal viewing through browser.

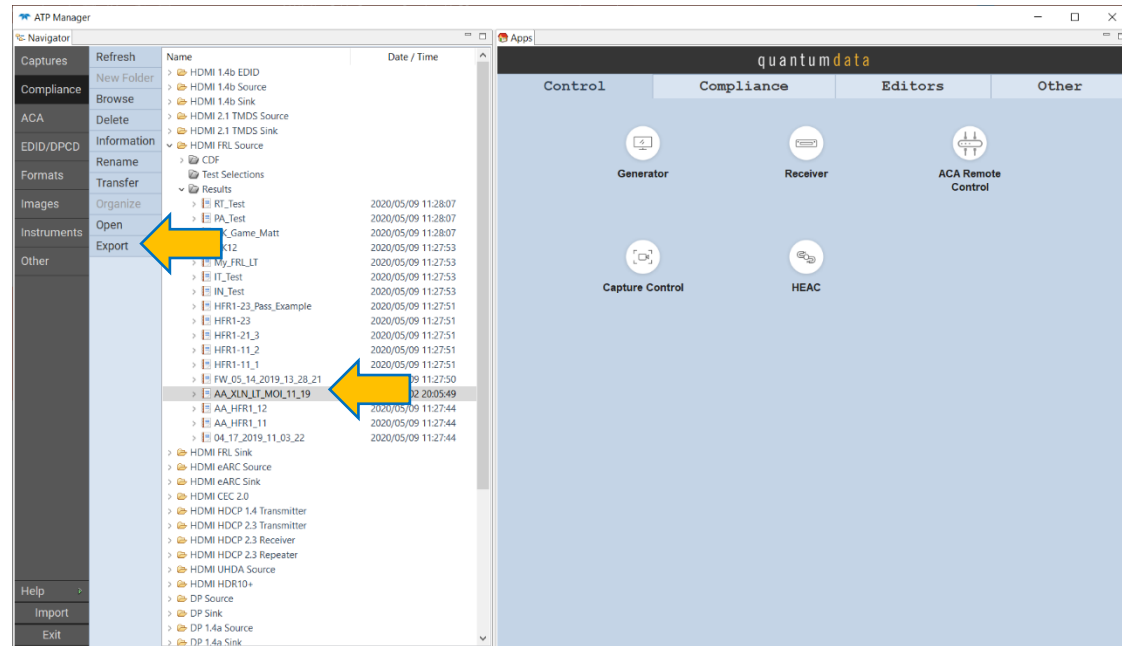
The screenshot shows an HTML Viewer window displaying test results for two tests: Test HFRL-11 and Test HFRL-19. Both tests are marked as 'Pass'.

Test Name	Source	Overall Result
Test HFRL-11	Source FRL Protocol - Legal Codes	Pass
Iter 01: FRL 3 Lane Mode	Trained at: (2) 6 Gbps @ 3 Lanes	Pass
01: Test that the FRL characters count and SSB-SR characters count is valid.	Pass	
02: SR header occurs only after 32 super blocks and at SB count '0'.	Pass	
03: Illegal codes or other related errors associated with this test case.	Pass	
04: SSB/SR header occurs only prior to Character block '0'.	Pass	
Iter 02: FRL 4 Lane Mode	Trained at: (5) 10 Gbps @ 4 Lanes	Pass
01: Test that the FRL characters count and SSB-SR characters count is valid.	Pass	
02: SR header occurs only after 32 super blocks and at SB count '0'.	Pass	
03: Illegal codes or other related errors associated with this test case.	Pass	
04: SSB/SR header occurs only prior to Character block '0'.	Pass	
Test HFRL-19	Source FRL Packets - FRL Map Characters	Pass
Iter 01: Lowest FRL Rate in 3 Lane mode	Trained at: (2) 6 Gbps @ 3 Lanes	Pass
01: Test that the FRL MAP Type is valid.	Pass	
02: Test that Video Blanking/Video Data Characters Length is greater than 1	Pass	
03: Test That the sum of all MAP Length fields in a Super Block is 2008.	Pass	
Iter 02: Lowest FRL Rate in 4 Lane mode		

Compliance Testing – Export Compliance Test Results

◆ HDMI Aux Compliance Test Results Export:

- ◆ Save compliance test results and HTML file for easy and universal viewing through browser.
- ◆ Export compliance test results for dissemination to colleagues, other subject matter experts or Teledyne Customer Support.



HDMI 2.1 Source Testing

HDCP Compliance Testing

HDMI - HDCP 2.3 Source Compliance Testing

◆ HDMI HDCP 2.3 compliance Testing:

- ◆ Run HDCP 2.3 source compliance tests. All tests supported.
- ◆ Run HDCP 2.3 repeater tests. All tests supported.
- ◆ Provides detailed Test Results with Pass/Fail and details for each subtest.
- ◆ Enables compliance self-testing and/or pre-testing of HDMI devices.
- ◆ Enables export compliance test results to share with colleagues.

Compliance Test Results Viewer

DP HDCP 2.2 Receiver (1.0) Compliance Test Results

Results Name: AA_Com_Monitor_1 Manufacturer: LG
Date Tested: March 15, 2017 7:57 PM Model Name: 5K Monitor
Overall Status: **CTS 1.0 - Pass** Port Tested: 1

HTML Report

Test Name / Details	Status
2C-01: Regular Procedure - With transmitter	Pass
Iter 01: With previously not connected receiver	Pass
Iter 02: With previously connected receiver	Pass
TX:HPD::ENTER	
TX HPD:**Test Cond.** auth	
TX UNAUTH::ENTER	
TX MSGR:Disable ENC_EN ts:3957204961.28 us	
TX UNAUTH:AKE_INIT ts:3958706882.56 us	
TX UNAUTH:MSG RD:AKE_Init ts:3958706882.56 us	
TX UNAUTH:MSG RCVD:AKE_Send_Cert ts:3958759403.52 us	
TX UNAUTH:Rrx 0,7f,d4,f0,cf,b3,4c,86	
TX UNAUTH:RxCaps 2 0 2	
TX AKE:Snd Stored_RM ts:3958786918.40 us	
TX AKE:MSG:AKE_Storage ts:3958786918.40 us	
TX AKE:MSG RCVD:AKE_Send_H_prime ts:3958822830.08 us	
TX LC:Snd LC_Init ts:3958824253.44 us	
TX LC:MSG:LC_Init ts:3958824253.44 us	
TX LC:MSG RCVD:LC_Send_L_prime ts:3958831534.08 us	
TX SKE:Snd SKE_Send_EKS ts:3958833356.80 us	
TX:AUTH::ENTER	
TX AUTH:Snd STRM_TYPE ts:3958843596.80 us 0	
TX MSGR:Enable ENC_EN ts:3959084165.12 us	
TX AUTH:MSG:SKE_Send_Eks ts:0.00 us	
Transmitted test pattern was visible on the Sink DUT.	
2C-02: Irregular Procedure - New Authentication after AKE Init	Pass
2C-03: Irregular Procedure - New Authentication during Locality Check	Pass
2C-04: Irregular Procedure - New Authentication after SKE Send Eks	Pass
2C-05: Irregular Procedure - New Authentication during Link Synchronization	Pass
2C-06: Regular Procedure - Encryption Disable Bootstrapping	Pass

Instrument: SS980B [10.30.196.70] Continue Test Execution

Close

HDMI HDCP 2.3 Source Compliance Testing

- ◆ HDMI HDCP 2.3 source compliance Testing:
 - ◆ Run HDCP 2.3 source compliance tests. All tests supported.
 - ◆ Run HDCP 2.3 repeater tests. All tests supported.
 - ◆ Provides detailed Test Results with Pass/Fail and details for each subtest.
 - ◆ Enables compliance self-testing and/or pre-testing of HDMI devices.
 - ◆ Enables export compliance test results to share with colleagues.

Compliance Test Results Viewer

HDMI HDCP 2.3 TX (1.0) Compliance Test Results

Results Name: AA_HDMI_HDCP_22_PC Manufacturer: Nvidia
Date Tested: May 17, 2016 3:57 PM Model Name: GTX
Overall Status: **CTS 1.0 - Fail** Port Tested: 1

HTML Report

Test Name / Details	Status
1A-01: Regular Procedure: With previously connected Receiver (With stored Km)	Pass
Iter 01:	Pass
1A-02: Regular Procedure: With newly connected Receiver (Without stored Km)	Pass
1A-03: Regular Procedure: Receiver disconnect after AKE Init	Pass
1A-04: Regular Procedure: Receiver disconnect after Km	Pass
1A-05: Regular Procedure: Receiver disconnect after locality check	Pass
1A-06: Regular Procedure: Receiver disconnect after Ks	Fail
Iter 01:	Fail
Clear Ready	
RX HPD Deasserted regular ts:5115282636.80 us	
RX HPD Asserted regular ts:5115432673.28 us	
RX UNAUTH::ENTER	
RX UNAUTH:HDMI/VIDEO Present	
RX UNAUTH:MSG RD:ENC_DIS ts:5115992064.00 us	
RX UNAUTH:RCVD:AKE_Init ts:0.00 us	
RX UNAUTH:**Test Cond.** hpd	
RX AKE:MSG SND:AKE_Send_Cert ts:5117223004.16 us	
RX AKE:MSG RCVD:AKE_No_Stored_km ts:5118022901.76 us	
RX PAIR::ENTER	
RX PAIR:MSG RD:AKE_Send_H_Prime ts:5118037442.56 us	
RX LC:MSG SND:AKE_Send_Pairing_Info ts:5118050856.96 us	
RX LC:MSG RCVD:LC_Init ts:5118052044.80 us	
RX LC:MSG SND:LC_Send_L_prime ts:5118058301.44 us	
RX LC:MSG RCVD:SKE_Send_Eks ts:5118072350.72 us	
RX SKE::ENTER	
RX SKE:MSG RCVD:SKE_Send_Eks ts:5118072350.72 us	
RX HPD Deasserted irregular ts:5118072606.72 us	
RX HPD Asserted irregular ts:5118272634.88 us	
RX UNAUTH:MSG RD:ENC_EN ts:5118292039.68 us	
Encryption Enabled	
1A-07: Regular Procedure: Receiver sends REAUTH REQ after Ks	Pass
1A-08: Irregular Procedure: Rx certificate not received.	Pass

Instrument: SS980B [10.30.196.70] Continue Test Execution

Close

HDMI HDCP 2.3 Source Compliance Test - ACA Test Capture Logs

◆ HDMI Aux Channel Analyzer Timestamp control:

- ◆ View the ACA transaction files for each HDCP test to confirm failures.
- ◆ View details of any transaction.
- ◆ View time stamps.

The screenshot shows the ACA Data Viewer interface. The main window displays a list of transactions from 1441 to 1477. Transaction 1455 is highlighted in blue. A yellow arrow points from the transaction list to the detailed view on the right. The detailed view shows the following information:

- Start Time: +02:04:16.338477
- Type: Native
- Direction: Request
- Command: Read
- Address: 0x692F8 (L')
- Length: 8
- [0000][96 92 F8 07 -- -- -- --][...]

The transaction list shows the following details for transaction 1455:

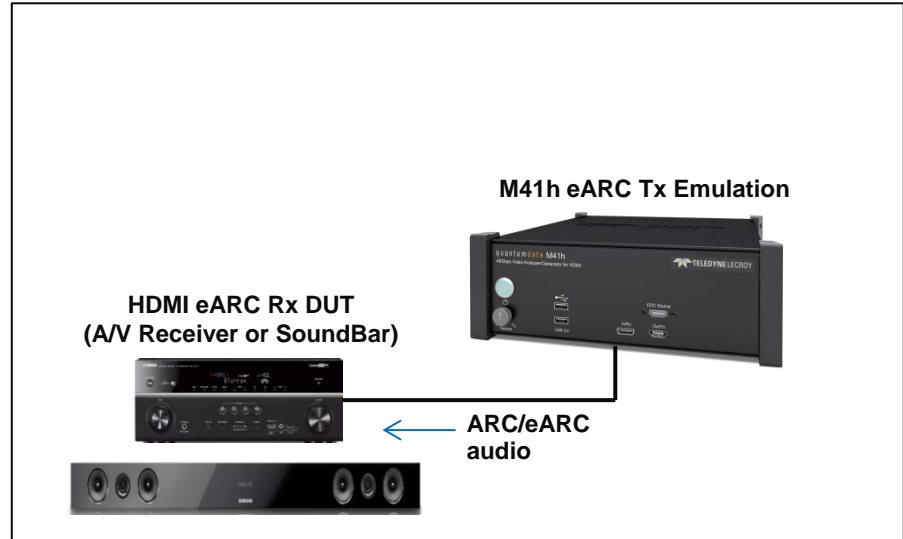
Transaction ID	Type	DP	Timestamp	Direction	Details
1455	DHDCP	DP-T61	+02:04:16.338477	>	R: 692F8 L' L=8

HDMI 2.1 eARC Rx Testing

Enhanced Audio Return Channel

HDMI eARC Rx Testing

- ◆ HDMI 2.1 eARC Testing:
 - ◆ Verify eARC Rx (e.g. Sound Bar) for common mode and differential mode operation.
 - ◆ Run eARC common and differential mode compliance tests for Rx devices. Full list of tests.



HDMI eARC Rx Testing

- ◆ HDMI 2.1 eARC Testing:
 - ◆ Verify eARC Rx (e.g. Sound Bar) for common mode and differential mode operation.
 - ◆ Run eARC common and differential mode compliance tests for Rx devices. Full list of tests supported (only partial list shown right).



HDMI eARC Rx Testing

- ◆ HDMI 2.1 eARC Testing:
 - ◆ Verify eARC Rx (e.g. Sound Bar) for common mode and differential mode operation.
 - ◆ Run eARC common and differential mode compliance tests for Rx devices. Full list of tests supported.
 - ◆ Provides detailed Test Results with Pass/Fail and details for each subtest.
 - ◆ Enables compliance self-testing and/or pre-testing of eARC devices.
 - ◆ Enables export of compliance test results to share w/ colleagues.

Compliance Test Results Viewer

eARC Sink (1.0) Compliance Test Results

Results Name: AA_eARC_Rx_Complete_MB Manufacturer: Lattice
Date Tested: August 13, 2018 11:14 AM Model Name: eval
Overall Status: **CTS 1.0 - Fail** Port Tested: 1

Test Results

Test Name / Details	Status
▶ HFR5-2-20: eARC Discovery With COMMA Response Margining	Pass
▲ HFR5-2-21: Command Behavior With Bit Time Margining	Pass
Iter 01:	Pass
▶ 01: HFR5 2 21 1: Shortest Bit Time, Earliest Middle Edge	Pass
▶ 02: HFR5 2 21 2: Shortest Bit Time, Latest Middle Edge	Pass
▶ 03: HFR5 2 21 3: Longest Bit Time, Earliest Middle Edge	Pass
▶ 04: HFR5 2 21 4: Longest Bit Time, Latest Middle Edge	Pass
Iteration 4, Longest Bit Time, Latest Middle Edge	
Collecting data for 7000ms	
Collected 2738 events	
Analyzed 2618 events	
TeARC_RX_CONN_START: 20.8082ms (maximum: 200ms)	
COMMA ON #1 was measured at 9.9631ms	
COMMA OFF #1 was measured at 9.9518ms	
COMMA ON #2 was measured at 9.96405ms	
COMMA OFF #2 was measured at 9.951425ms	
COMMA ON #3 was measured at 9.96345ms	
870 packets analyzed	
Re-analyzed 2738 events	
eARC_Read 0x74/0xD2=0x28	
eARC_Write 0x74/0xD3=0x00	
▶ HFR5-2-22: Behavior if no response to eARC Discovery	Pass
▶ HFR5-2-23: eARC RX gets Unexpected Device ID	Pass
▶ HFR5-2-24: eARC RX gets new Opcode in the middle of a Command	Pass
▶ HFR5-2-25: eARC RX gets Heartbeat Disconnect	Pass
▶ HFR5-2-26: eARC RX gets HPD LOW during eARC Discovery	Pass

Open ACA Data HFR5-2-20: eARC Discovery With COMMA Response Margining

Instrument: SS980B [10.30.196.240] Continue Test Execution

Close

HDMI eARC Common Mode Configuration Sequence

- ◆ HDMI 2.1 eARC Testing:
 - ◆ Verify eARC common mode connection sequence using Aux Channel Analyzer (ACA) utility.
 - ◆ Enables export of ACA eARC Common Mode transactions to share w/ colleagues.

ACA Data Viewer

Open Close Export Options Filter Find

[My_eARC_Log_1] Events: 28 (54)

Time	Type	Channel	Time	Description
0	EARC	HDMI-R10	+06:37:28.021241	Invalid Sequence
1	EARC	HDMI-R10	+06:37:28.069262	Read EARC_RX_STAT 00
2	EARC	HDMI-R10	+06:37:28.069813	Write EARC_TX_STAT 81
3	EARHB	HDMI-R10	+06:37:28.116296	Heartbeats 166
4	SV	HDMI-R10	+06:37:36.078772	SV Falling Edge
5	SV	HDMI-R10	+06:37:37.884404	SV Rising Edge
6	EARCM	HDMI-R10	+06:37:37.885490	Comma CN: 9.999 ms
7	EARCM	HDMI-R10	+06:37:37.905489	Comma CN: 10.000 ms
8	EARCM	HDMI-R10	+06:37:37.925489	Comma CN: 10.000 ms
9	EARC	HDMI-R10	+06:37:37.939303	Read EARC_RX_STAT 18
10	EARC	HDMI-R10	+06:37:37.939853	Write EARC_TX_STAT 99
11	EARHB	HDMI-R10	+06:37:37.985256	Heartbeats 1
12	EARC	HDMI-R10	+06:37:38.033313	Read EARC_RX_STAT 00
13	EARC	HDMI-R10	+06:37:38.033860	Write EARC_TX_STAT 81
14	EARC	HDMI-R10	+06:37:38.081215	Read CAPS 00h L=8
15	EARCD	HDMI-R10	+06:37:38.082492	Cap Data: L=8
16	EARC	HDMI-R10	+06:37:38.082526	Read ERX_LATENCY 00
17	EARHB	HDMI-R10	+06:37:38.083075	Heartbeats 27
18	EARC	HDMI-R10	+06:37:39.392340	Read EARC_RX_STAT 00
19	EARC	HDMI-R10	+06:37:39.392909	*Write EARC_TX_STAT 81
20	EARHB	HDMI-R10	+06:37:39.440367	Heartbeats 37
21	EARC	HDMI-R10	+06:37:41.228225	Read EARC_RX_STAT 00
22	EARC	HDMI-R10	+06:37:41.228761	Write EARC_TX_STAT
23	EARHB	HDMI-R10	+06:37:41.277215	Heartbeats 43
24	EARC	HDMI-R10	+06:37:43.341254	Read EARC_RX_STAT 00
25	EARC	HDMI-R10	+06:37:43.341835	Write EARC_TX_STAT
26	EARHB	HDMI-R10	+06:37:43.389271	Heartbeats 83
27	EARC	HDMI-R10	+06:37:47.396808	Write

Type: eArc
Start Time: +06:37:38.033313
Duration: 514 us

Read EARC_RX_STAT 00

0xDO: EARC_RX_STAT

Bit	Name	Value	Description
0	EARC_HPD	N(0)	
1		0	Reserved
2		0	Reserved
3	CAP_CHNG	N(0)	
4	STAT_CHNG	N(0)	
5		0	Reserved
6		0	Reserved
7		0	Reserved

Packet Sequence:

001:	M	C	01h	Read	+0 us
002:	S	C	04h	Ack	+24 us
003:	M	D	74h		+34 us
004:	S	C	04h	Ack	+24 us
005:	M	D	D0h		+34 us
006:	S	C	04h	Ack	+24 us
007:	M	C	10h	Cont	+31 us
008:	S	D	00h		+24 us
009:	M	C	20h	Stop	+34 us
010:	S	C	04h	Ack	+24 us

(M/S = Master/Slave, C/D = Command/Data)

12: Read EARC_RX_STAT 00

HDMI 2.1 Sink Testing Video Generation

HDMI 2.1 Video Generator Function – Select Resolution and Color Parameters

- ◆ HDMI Video Generator:
 - ◆ Test 4K and 8K UHD TVs with a variety of video formats and colorimetry settings.

The screenshot shows the 'Generator' software interface. At the top, the 'Modes' section displays 'MODE: FRL FRL: 4/10G FMT: 4320p60' with a yellow arrow pointing to it. Below this, a status bar shows '(199) 7680x4320p @ 60 Hz 16:9' and '7680x4320 Progressive YCbCr-420: BT.2020-YCC-10bpc'. The main interface is divided into several sections: 'Format' (CTA, VESA, Folder, Lists, EDID), 'Pattern', 'Audio', and 'Tools'. A table lists various resolutions and their parameters. A yellow arrow points to the '4320p' row in the 'Resolution' column. Another yellow arrow points to the '4320p60 VIC 199' button in the 'Aspect Ratio' section. The bottom of the interface includes 'Left to Right', 'Settings', 'Edit', 'Clear Selection', and a 'CLOSE' button.

Resolution	Vtotal	Frame Rate	Aspect Ratio
240p2x 240p4x	262 263	24/1.001 24	4:3
288p2x 288p4x	312 313		16:9
480p	314	30/1.001 30	64:27
480p2x 480i2x		48/1.001 48	256:135
480p4x 480i4x			50
576p		60/1.001 60	Box FILL
576p2x 576i2x			100
576p4x 576i4x		120/1.001 120	4:3
720p			16:9
1080p 1080i	1125 1250	240/1.001 240	1.85:1
4320p			2.39:1

HDMI 2.1 Video Generator Function – Select Resolution and Color Parameters

- ◆ HDMI Video Generator:
 - ◆ Test 4K UHD TVs with a variety of video formats and video parameters.
 - ◆ Use variety of test patterns including moving patterns to check motion artifacts.
 - ◆ Extensive video format library with the ability to create custom formats.

The screenshot shows the 'Generator' software interface. At the top, it displays 'Modes' with details: MODE: FRL, FRL: 4/10G, FMT: 4320p60, P-Rate: 1485.00MHz, F-Rate: 60.00Hz, INTF: HDMI, DSC: No, IMG: SmpteBar, H-Rate: 264.00kHz, and Output. Below this is a table of video formats with columns for CTA, VESA, Folder, Lists, EDID, and a 'Box FILL' column. A yellow arrow points to the '4320p60 VIC 199' format. A 'Format Settings' dialog box is open, showing 'Color Space' options (RGB, YCbCr, xvYCC, opRGB, sYCC601, opYCC, BT2020 cYCC, BT2020 YCC, BT2020 RGB, DCI-P3) with 'BT2020 YCC' selected. Below that, 'Range' options (Full, Shoot, Limited) are shown with 'Limited' selected. 'Bits per Component' options (8, 10, 12, 16) are shown with '10' selected. A 'Scrambling Override' section shows 'Scrambling Currently Enabled' with 'Enabled' selected. A yellow arrow points to the '4:2:0' color subsampling option. At the bottom of the dialog is an 'APPLY' button.

Resolution	Vtotal	Frame Rate	Box FILL
240p2x 240p4x	262 263	24/1.001 24	4:3
288p2x 288p4x	312 313	30/1.001 30	16:9
480p	314	48/1.001 48	64:27
480p2x 480i2x		50	256:135
480p4x 480i4x		60/1.001 60	Box FILL
576p		100	4:3
576p2x 576i2x		120/1.001 120	16:9
576p4x 576i4x		240/1.001 240	1.85:1
720p			2.39:1
1080p 1080i	1125 1250		
2160p 4320p			

HDMI TMD5 Video Generation – Configure Outgoing Metadata

- ◆ HDMI Video Generator:
 - ◆ Test 4K UHD TVs with a variety of video formats and video parameters.
 - ◆ Enables user control over Infoframe and data island transmission for irregular testing.

The screenshot shows the 'Generator' application window. At the top, it displays video mode information: (199) 7680x4320p @ 60 Hz 16:9, 7680x4320 Progressive YCbCr-420: BT.2020-YCC-10bpc. The interface is divided into several sections: 'Format', 'Pattern', 'Audio', and 'Tools'. A yellow arrow points to the 'Tools' tab. Below this, there are sections for 'EDID Decode', 'EDID Comp', and 'Editors'. A yellow arrow points to the 'InfoFrame' option in the 'Editors' list. The main area shows configuration options for the 'InfoFrame', including 'Video Format ID (VIC): 0', 'Component Format (Y): 0 = RGB', 'AFD Present (A): 0 = No', 'Bar Data (B): 0 = Not Present', 'Scan Info (S): 1 = Overscanned', 'Colorimetry (C): 1 = SMPTE 170M [1]', 'Picture Aspect Ratio (M): 0 = No Data', 'Active Aspect Ratio (R): 0 = Not Specified', 'ITC Content (ITC): 0 = No Data', 'Ext. Colorimetry (EC): 0 = xvYCC601', 'RGB Quantization (Q): 0 = Default', 'Picture Scaling (SC): 0 = None', 'YCC Quantization (YQ): 0 = Limited Range', 'IT Content Type (CN): 0 = Graphics', and 'Pixel Repetition (PR): 0 = No Repetition (x1)'. At the bottom, there is a table for 'Add. Colorimetry Ext (ACE)' with columns for T, V, L, C, Params 1, VIC, Params 2, and AFD. The table contains the following data:

T	V	L	C	Params 1	VIC	Params 2	AFD
82	02	0D	2E	014000	00	00	0000000000000000

Below the table, there is a section for 'Params 3' with a 'Reserved' column and a value of '00' followed by a long string of zeros.

HDMI Video Generator Function

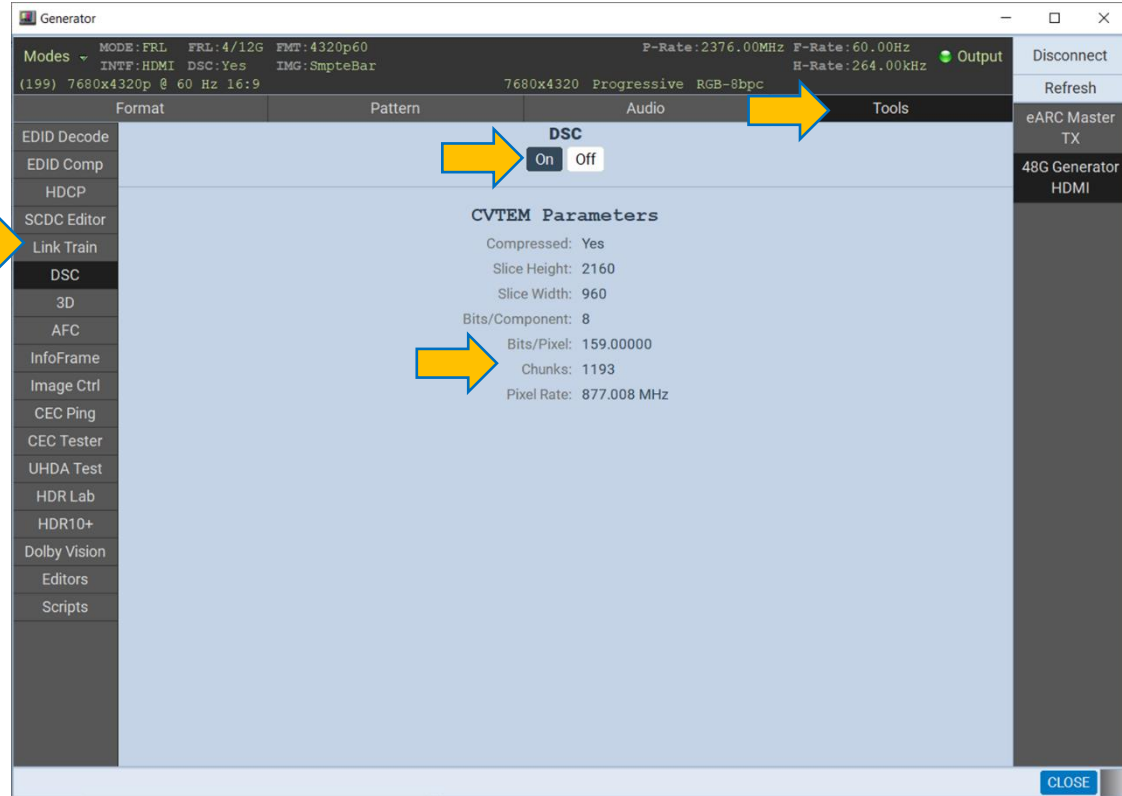
- ◆ HDMI Video Generator:
 - ◆ Test 4K and 8K UHD TVs with a variety of video formats and colorimetry settings.
 - ◆ Configure Link settings with Lane rate & number of Lanes.
 - ◆ Turn FRL Off to test TMDS.

The screenshot shows the 'Generator' application window. At the top, it displays various settings: MODE: FRL, FRL: 4/10G, FMT: 4320p60, F-Rate: 1485.00MHz, F-Rate: 60.00Hz, INTF: HDMI, DSC: No, IMG: SmpteBar, H-Rate: 264.00kHz, and an 'Output' indicator. Below this, it shows video format details: (199) 7680x4320p @ 60 Hz 16:9, 7680x4320 Progressive YCbCr-420: BT.2020 VCC-10bpc. The main interface is divided into sections: 'Format', 'Pattern', 'Audio', and 'Tools'. The 'Link Train' section is active, showing 'Current Status' with State: LTS_P, Lanes: 4, Rate: 10 GHz, FFE: 0, and FRL PLL LOCKED: YES. To the right, the 'Force Link Train at' section lists options for Lane / Rate: FRL Off, 3 Lanes / 3 Gbps, 3 Lanes / 6 Gbps, 4 Lanes / 6 Gbps, 4 Lanes / 8 Gbps, 4 Lanes / 10 Gbps, and 4 Lanes / 12 Gbps. A 'CLOSE' button is at the bottom right. Yellow arrows point to the 'Link Train' menu item, the 'Tools' tab, and the '4 Lanes / 10 Gbps' option.

HDMI Video Generator Function – Selecting DSC

◆ HDMI Video Generator:

- ◆ Test 4K and 8K UHD TVs with a variety of video formats and colorimetry settings.
- ◆ Configure Link settings with Lane rate & number of Lanes.
- ◆ Turn FRL Off to test TMDS.
- ◆ You can active Display Stream Compression (DSC) when the M41h is in the FRL video generation mode.



HDMI Video Generator Function – DSC Image Caching

◆ HDMI Video Generator – DSC Image Caching:

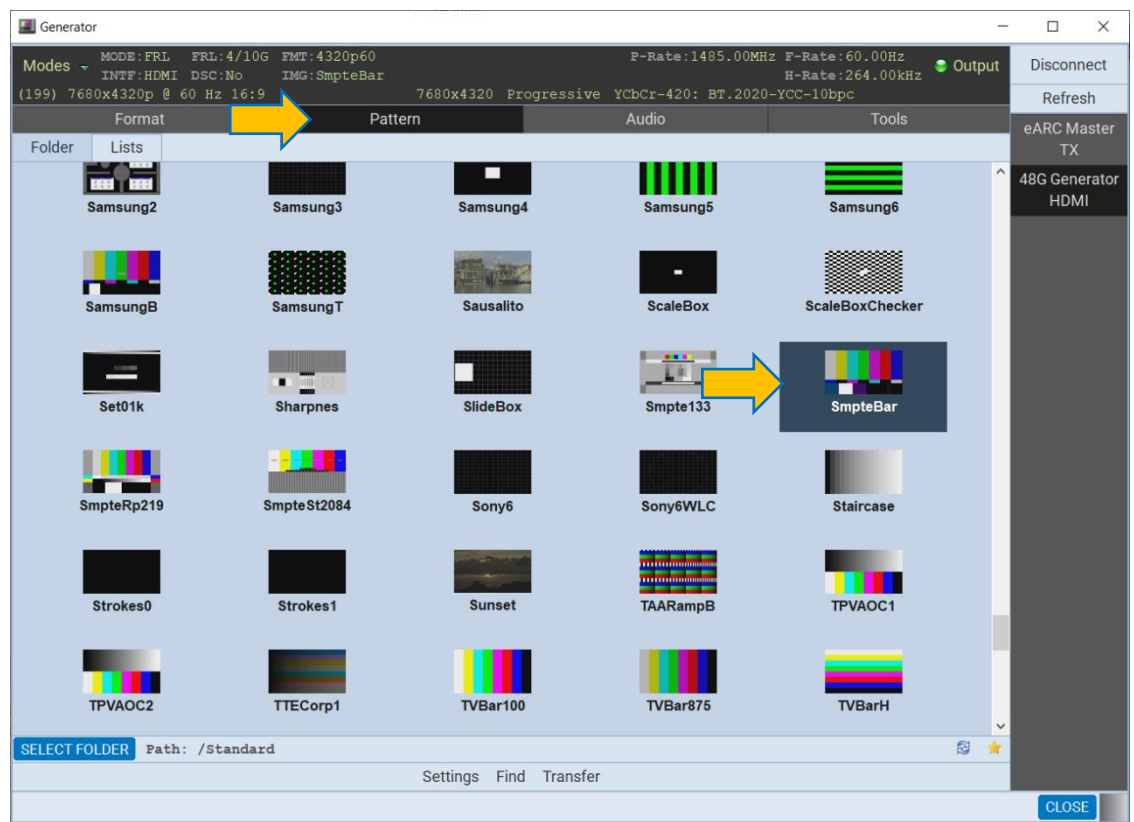
- ◆ Install or create cached, pre-compressed DSC images for quick rendering.

The screenshot displays the software interface for the HDMI Video Generator. The 'DSC' tab is selected, and the 'Cache' sub-tab is active. A yellow arrow points from the 'Cache' sub-tab to the 'ADD CURRENT DSC IMAGE TO THE CACHE' button. Another yellow arrow points from the 'DSC' sub-tab in the left-hand menu to the main content area. The interface shows a list of DSC images with columns for ID, Master, Format, and Bpp. The 'Cache' sub-tab contains two buttons: 'ADD CURRENT DSC IMAGE TO THE CACHE' and 'REMOVE SELECTED IMAGE FROM THE CACHE'.

ID	Master	Format	Bpp
01	Master	3840x2160, YCbCr 4:2:0, 10 bpc, Slice 1520x2160, 24	
02	Master	3840x2160, YCbCr 4:2:0, 12 bpc, Slice 1920x2160, 24	bpp
03	Master	4096x2160, YCbCr 4:2:0, 10 bpc, Slice 2048x2160, 24	bpp
04	Master	4096x2160, YCbCr 4:2:0, 12 bpc, Slice 2048x2160, 24	bpp
05	Master	3840x2160, YCbCr 4:2:0, 8 bpc, Slice 1920x2160, 17.125	bpp
06	Master	3840x2160, YCbCr 4:2:0, 10 bpc, Slice 1920x2160, 17.125	bpp
07	Master	3840x2160, YCbCr 4:2:0, 12 bpc, Slice 1920x2160, 17.125	bpp
08	Master	3840x2160, YCbCr 4:2:0, 8 bpc, Slice 1920x2160, 14.125	bpp
09	Master	3840x2160, YCbCr 4:2:0, 10 bpc, Slice 1920x2160, 14.125	bpp
10	Master	3840x2160, YCbCr 4:2:0, 12 bpc, Slice 1920x2160, 14.125	bpp
11	Master	4096x2160, RGB 4:4:4, 12 bpc, Slice 2048x2160, 12	bpp
12	Master	5120x2160, YCbCr 4:2:0, 8 bpc, Slice 2560x2160, 24	bpp
13	Master	5120x2160, YCbCr 4:2:0, 10 bpc, Slice 2560x2160, 24	bpp
14	Master	5120x2160, YCbCr 4:2:0, 8 bpc, Slice 2560x2160, 24	bpp
15	Master	5120x2160, YCbCr 4:2:0, 8 bpc, Slice 2560x2160, 21.625	bpp
16	Master	5120x2160, YCbCr 4:2:0, 10 bpc, Slice 2560x2160, 21.625	bpp
17	Master	5120x2160, YCbCr 4:2:0, 12 bpc, Slice 2560x2160, 21.625	bpp
18	Master	5120x2160, YCbCr 4:2:0, 8 bpc, Slice 1280x2160, 24	bpp
19	Master	5120x2160, YCbCr 4:2:0, 10 bpc, Slice 1280x2160, 24	bpp
20	Master	5120x2160, YCbCr 4:2:0, 12 bpc, Slice 1280x2160, 24	bpp
21	Master	5120x2160, YCbCr 4:2:0, 8 bpc, Slice 1280x2160, 21.875	bpp
22	Master	3840x2160, RGB 4:4:4, 10 bpc, Slice 960x2160, 12	bpp
23	Master	5120x2160, YCbCr 4:2:0, 10 bpc, Slice 1280x2160, 21.875	bpp
24	Master	5120x2160, YCbCr 4:2:0, 12 bpc, Slice 1280x2160, 21.875	bpp
25	Master	4096x2160, YCbCr 4:2:0, 8 bpc, Slice 2048x2160, 16.125	bpp
26	Master	4096x2160, YCbCr 4:2:0, 10 bpc, Slice 2048x2160, 16.125	bpp
27	Master	4096x2160, YCbCr 4:2:0, 12 bpc, Slice 2048x2160, 16.125	bpp
28	Master	4096x2160, YCbCr 4:2:0, 8 bpc, Slice 2048x2160, 13.25	bpp
29	Master	4096x2160, YCbCr 4:2:0, 10 bpc, Slice 2048x2160, 13.25	bpp
30	Master	4096x2160, YCbCr 4:2:0, 12 bpc, Slice 2048x2160, 13.25	bpp
31	Master	7680x4320, YCbCr 4:2:2, 12 bpc, Slice 960x4320, 16.75	bpp
32	Master	7680x4320, YCbCr 4:2:2, 12 bpc, Slice 960x4320, 16.75	bpp

HDMI Video Generator Function – Test Pattern Selection

- ◆ HDMI Video Generator:
 - ◆ Test 4K and 8K UHD TVs with a variety of video formats and colorimetry settings.
 - ◆ Includes a variety of test patterns and special patterns for testing UHD displays.
 - ◆ Verify HDR rendering capabilities of a 8K UHD TV.



HDMI Video Generator Function – HDR Test Patterns

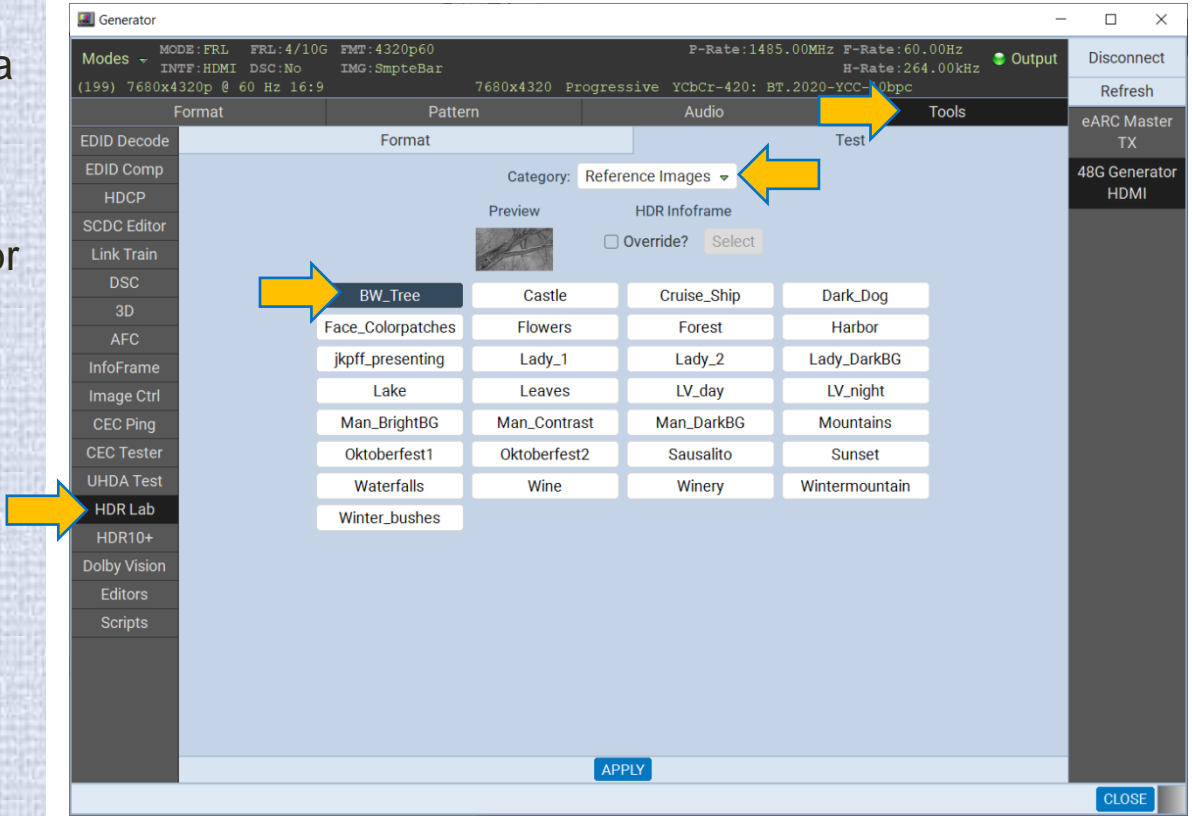
- ◆ HDMI Video Generator:
 - ◆ Test 4K and 8K UHD TVs with a variety of video formats and colorimetry settings.
 - ◆ Includes a variety of test patterns and special patterns for testing UHD displays.
 - ◆ Verify HDR rendering capabilities of a 4K and 8K UHD TV.

The screenshot shows the 'Generator' software interface. At the top, it displays system information: MODE: FRL, FRL: 4/10G, FMT: 4320p60, P-Rate: 1485.00MHz, F-Rate: 60.00Hz, INTF: HDMI, DSC: No, IMG: SmpteBar, H-Rate: 264.00kHz, and Output status. Below this, it shows the current format: (199) 7680x4320p @ 60 Hz 16:9, 7680x4320 Progressive, YCbCr-420: BT.2020-YCC-10bpc. A yellow arrow points to the 'Audio' tab in the top navigation bar. The main area is titled 'Select a 2160p/BT2020 Mode' and contains a table of options. A yellow arrow points to the 'HDR Lab' option in the left sidebar. The 'Depth' dropdown is set to '10 bpc'. An 'APPLY' button is at the bottom center, and a 'CLOSE' button is at the bottom right.

RGB	YCC-420	YCC-422	YCC-444
23 Hz	50 Hz	23 Hz	50 Hz
24 Hz	59 Hz	24 Hz	59 Hz
25 Hz	60 Hz	25 Hz	60 Hz
29 Hz		29 Hz	29 Hz
30 Hz		30 Hz	30 Hz

HDMI Video Generator Function – HDR Test Patterns

- ◆ HDMI Video Generator:
 - ◆ Test 4K and 8K UHD TVs with a variety of video formats and colorimetry settings.
 - ◆ Includes a variety of test patterns and special patterns for testing UHD displays.
 - ◆ Verify HDR rendering capabilities of a 8K UHD TV.



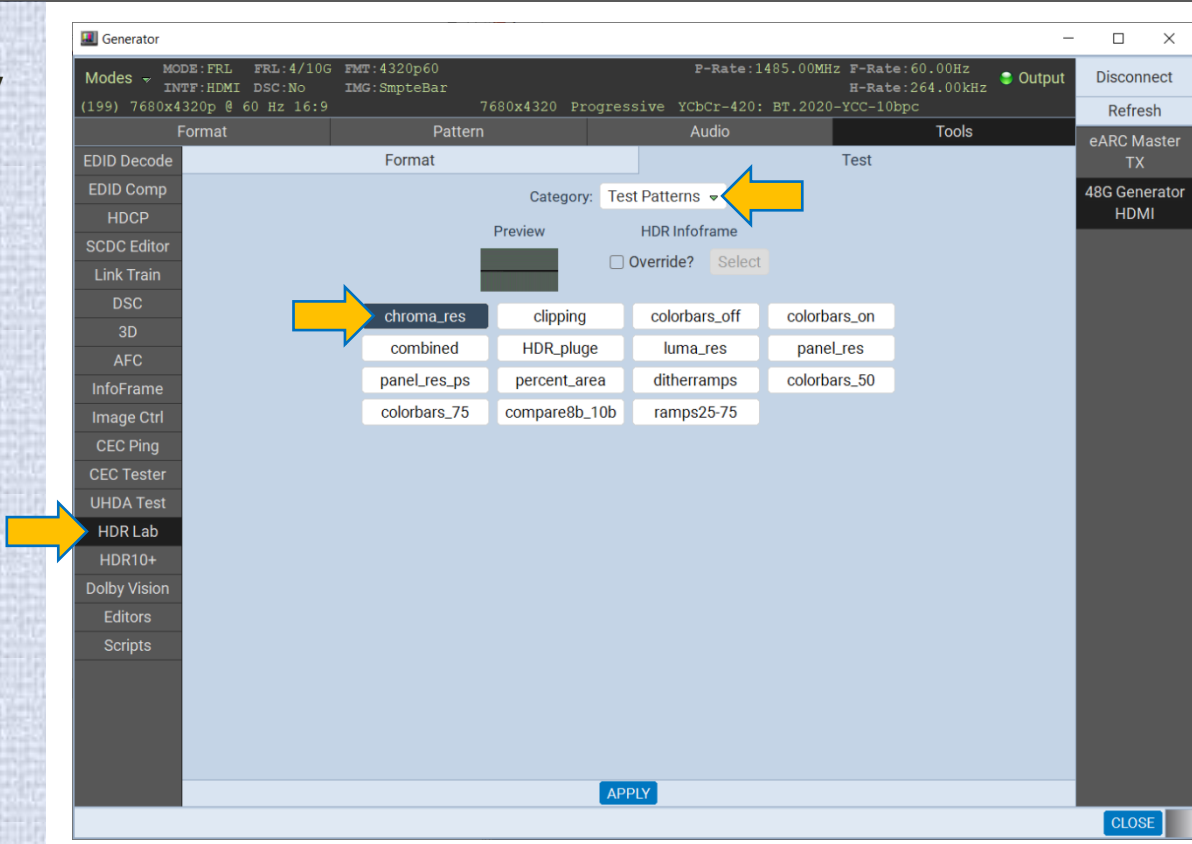
HDMI Video Generator Function – HDR Test Patterns

- ◆ HDMI Video Generator:
 - ◆ Test 4K and 8K UHD TVs for HDR10 with a variety of video formats and colorimetry settings.
 - ◆ Includes a variety of test patterns and special natural images (shown) for testing UHD displays.
 - ◆ Verify HDR rendering capabilities of 4K and 8K UHD TV for HDR10 subjectively.



HDMI FRL and TMDS Video Generation – HDR Lab

- ◆ HDMI Video Generator:
 - ◆ Test 4K UHD TVs with a variety of video formats and video parameters.
 - ◆ Verify HDR rendering capabilities of a 4K UHD TV for HDR10.



HDMI FRL Video Generation – HDR Lab

- ◆ HDMI Video Generator:
 - ◆ Test 8K UHD TVs with a variety of video formats and video parameters.
 - ◆ Verify HDR rendering capabilities of an 8K UHD TV for HDR10.

Format	Pattern	Audio	Tools
Link Train	1080p HDR	Format	Test
HDCP	4K HDR	Category: Reference Images	HDR InfoFrame
EDID Decode	8K HDR	Preview	
EDID Comp		Amsterdam_HDR_8k	
SCDC Editor		Heidelberg_HDR_8k	
DSC		LasVegas_HDR_8k	
3D		LosAngeles_HDR_8k	
AFC		Palnsee_HDR_8k	
InfoFrame		Zugspitze_HDR_8k	
Image Shift			
Image Ctrl			
CEC Ping			
CEC Tester			
UHDA Test			
HDR Lab			
HDR10+			
Dolby Vision			
Editors			
Scripts			

HDMI 2.1 Video Generator Function – HDR Test Patterns

- ◆ HDMI Video Generator:
 - ◆ Test 4K and 8K UHD TVs with a variety of video formats and colorimetry settings.
 - ◆ Includes a variety of HDR test patterns (shown) and special natural images for testing UHD displays.
 - ◆ Verify HDR rendering capabilities of a 4K and 8K UHD TV for HDR10 objectively.



HDMI Sink Testing

Custom Formats and Format Lists

Video Generator – Custom Format Timing

◆ HDMI Video Generator:

- ◆ Create custom video timings for testing a display's response to a variety of standard and non-standard or irregular timings.
- ◆ Save custom timings in separate list for easy access and testing.
- ◆ Create custom format lists of standard formats, e.g. 8K formats.

The screenshot shows the 'Format Editor' software interface with the 'Timing' tab selected. The window title is 'Format Editor: /User/My_Format'. The interface includes a menu bar with 'New', 'Open', 'Save', and 'Use'. Below the menu bar are tabs for 'Timing', 'General', 'Digital Video', 'Digital Audio', and 'AFD'. The main area is divided into several sections:

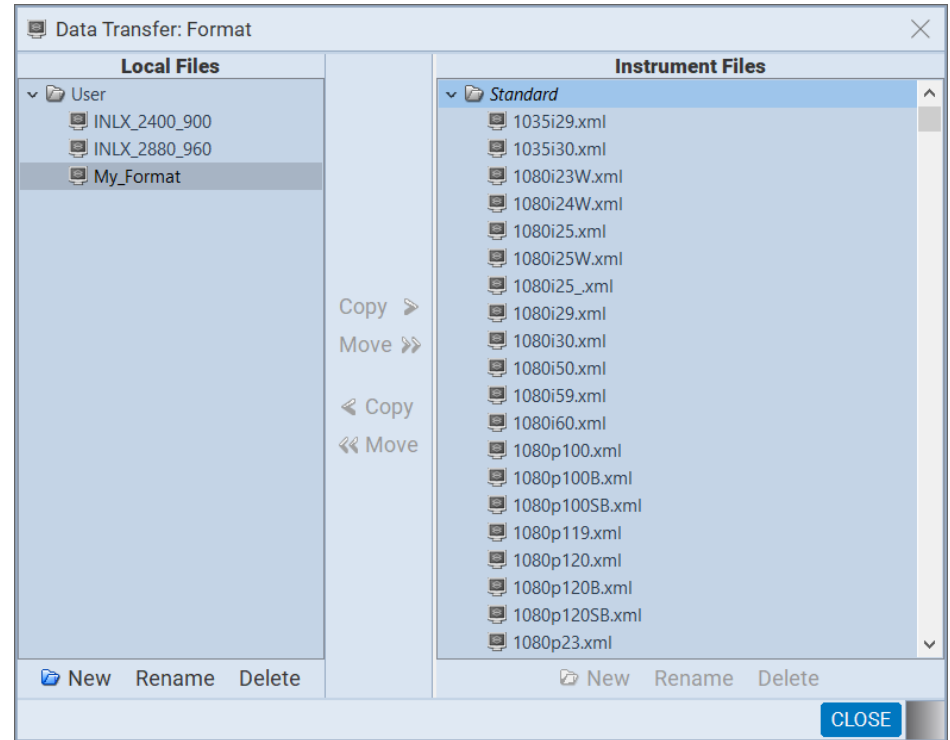
- Calculated:** Pixel Rate: 25.200000 KHz, 39.682540 ms.
- Rate:** 31.500000 KHz.
- Horizontal:** Rate: 31.500000 KHz, Tlines: 1.000000, Bases: 31.500000 KHz.
- Vertical:** Rate: 60.000000 Hz.
- Active:** 640 Pixels, 25.396825 us.
- Blank:** 160 Pixels, 6.349206 us.
- Total:** 800 Pixels, 31.746032 us.
- Pulse Delay:** 16 Pixels, 0.634921 us.
- Pulse Width:** 96 Pixels, 3.809524 us.
- Serration width Adjustment:** 0 Pixels.
- H to V Pulse Delay:** 0 Pixels.
- Horizontal Broad Pulse Delay:** 0 Pixels.
- Eq. Before:** 0 Lines.
- Eq. After:** 0 Lines.
- Entry Units:** Machine (selected), Time.
- Scan Type:** Progressive (selected), Interlace.
- Back Porch:** (unchecked).
- Clock Pulse:** (unchecked).
- PreEmphasis:** (unchecked).
- DC Balance:** (unchecked).
- Flat Front Porch:** (unchecked).
- TriLevel:** (unchecked).
- Repeat Field:** (unchecked).

A 'CLOSE' button is located at the bottom right of the window.

Video Generator – Custom Format Timing

◆ HDMI Video Generator:

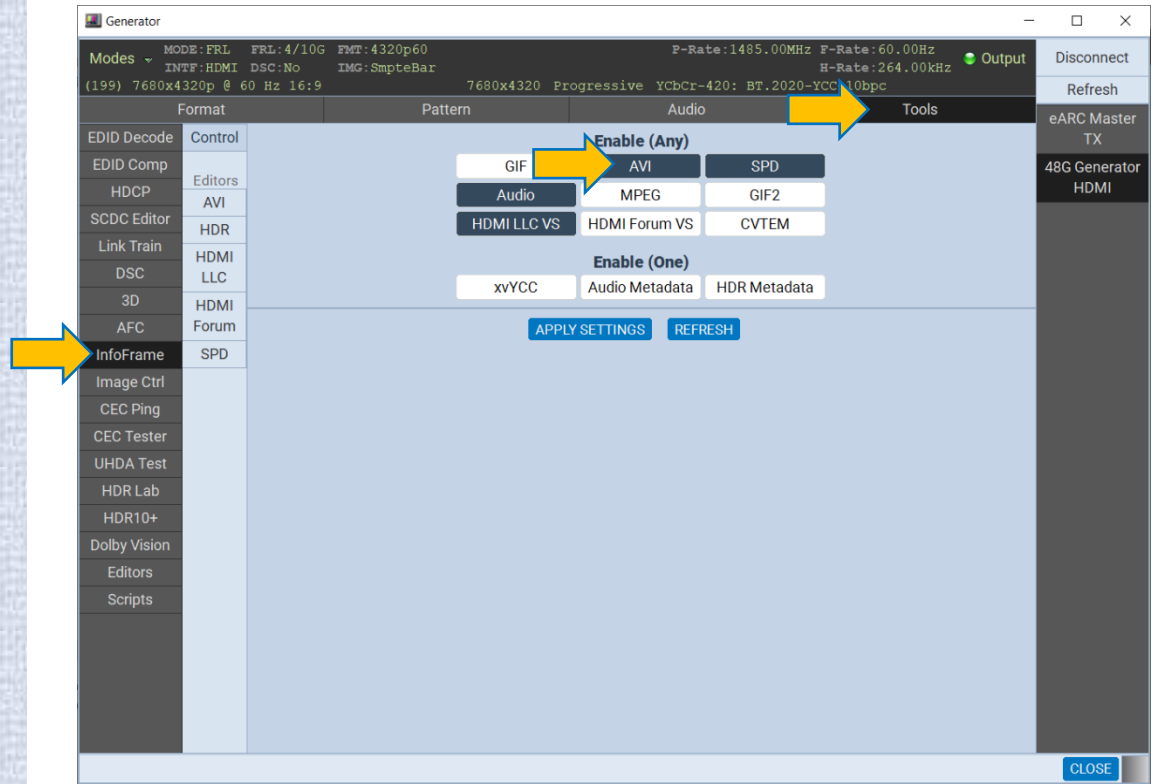
- ◆ Create custom video timings for testing a display's response to a variety of standard and non-standard or irregular timings.
- ◆ Save custom timings in separate list for easy access and testing.
- ◆ Create custom format lists of standard formats, e.g. 8K formats.



HDMI Sink Testing InfoFrame and Data Island Editor

HDMI Video Generator – Infoframe Output Control

- ◆ HDMI Video Generator:
 - ◆ Configure HDMI InfoFrame parameter values to test sink response to irregular conditions.
 - ◆ Examples show AVI InfoFrame and HDR InfoFrame.



HDMI Video Generator – Infoframe Output Control

- ◆ HDMI Video Generator:
 - ◆ Configure HDMI InfoFrame parameter values to test sink response to irregular conditions.
 - ◆ Example shows AVI InfoFrame.
 - ◆ Use Pull-Down menus to make changes to outgoing AVI InfoFrame.

Generator

Modes MODE: FRL FRL: 4/10G FMT: 4320p60 F-Rate: 1485.00MHz F-Rate: 60.00Hz Output
INTF: HDMI DSC: No IMG: SmpTeBar H-Rate: 264.00kHz
(199) 7680x4320p @ 60 Hz 16:9 7680x4320 Progressive YCbCr-420: BT.2020-YCC-10bpc

Format Pattern Audio Tools

EDID Decode Control New Open Save Read Write
EDID Comp Version: 2 3 4
Editors
AVI Video Format ID (VIC): 0 (0 - 255)
HDMI Component Format (Y): 0 = RGB
HDMI AFD Present (A): 0 = No
HDMI Bar Data (B): 0 = Not Present
HDMI Scan Info (S): 0 = No Data
HDMI Colorimetry (C): 2 = ITU-R BT.709 [7]
HDMI Picture Aspect Ratio (M): 0 = No Data
HDMI Active Aspect Ratio (R): 0 = Not Specified
HDMI ITC Content (ITC): 0 = No Data
HDMI Ext. Colorimetry (EC): 0 = xvYCC601
HDMI RGB Quantization (Q): 0 = Default
HDMI Picture Scaling (SC): 0 = None
HDMI YCC Quantization (YQ): 0 = Limited Range
HDMI IT Content Type (CN): 0 = Graphics
HDMI Pixel Repetition (PR): 0 = No Repetition (x1)
Add. Colorimetry Ext (ACE): 0 = DCL-P3 RGB (D65)

T	V	L	C	Params 1	VIC	Params 2	AFD
82	02	0D	EF	008000	00	00	0000000000000000
Params 3				Reserved			
00	0000000000000000000000000000						

CLOSE

Video Generator – HDMI InfoFrame Output Control

- ◆ HDMI Video Generator:
 - ◆ Configure HDMI InfoFrame parameter values to test sink response to irregular conditions.
 - ◆ Examples shows HDR InfoFrame.
 - ◆ Use fields to enter HDR parameters to outgoing HDR InfoFrame.

The screenshot displays the 'Generator' application window. The top status bar shows 'MODE: FRL', 'FRL: 4/10G', 'FMT: 4320p60', 'P-Rate: 1485.00MHz', 'F-Rate: 60.00Hz', 'INTF: HDMI', 'DSC: No', 'IMG: SmpteBar', 'H-Rate: 264.00kHz', and 'Output' status. Below this are tabs for 'Format', 'Pattern', 'Audio', and 'Tools'. The 'InfoFrame' tab is active in the left sidebar. The main panel shows the 'SPD' (Standard Parameter Data) configuration for the InfoFrame. It includes sections for 'Display Primaries' with x and y coordinates for x[0], x[1], x[2], y[0], y[1], and y[2], and 'Display Mastering Luminance' with 'max' and 'min' values. Two yellow arrows point to the 'Traditional gamma - SDR Luminance Range' and 'Traditional gamma - HDR Luminance Range' dropdown menus. At the bottom, there is a table for 'Static Metadata Descriptor' with columns T, V, L, C, EOTF, and SMD-ID, showing values like 87, 01, 1A, 5E, 00, and 00.

HDMI 2.1 Sink Testing Audio Generation

HDMI Audio Generator – LPCM Configuration

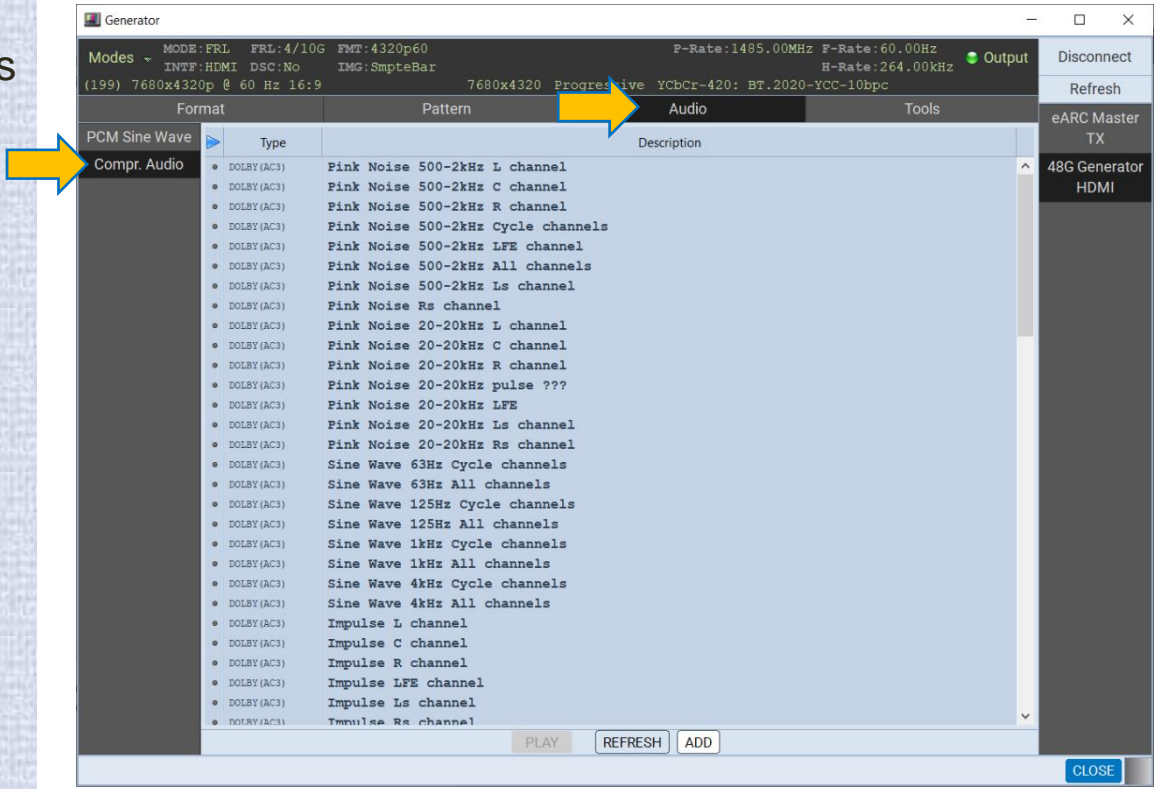
- ◆ HDMI Audio Generator:
 - ◆ Test UHD TVs and A/V receivers with a variety of audio formats.
 - ◆ Specify LPCM audio parameters in the sine wave such as number of channels, sampling rate, bits per pixel, and sine wave amplitude and frequency.



The screenshot shows the 'Generator' software window with the 'Audio' tab selected. The interface includes a top status bar with technical details like 'MODE: FRL', 'FRL: 4/10G', 'FMT: 4320p60', 'P-Rate: 1485.00MHz', 'F-Rate: 60.00Hz', 'INTF: HDMI', 'DSC: No', 'IMG: SmpteBar', '7680x4320', 'Progressive', 'YCbCr-420', 'BT.2020-YCC-10bpc', and 'Output' status. Below this, there are tabs for 'Format', 'Pattern', 'Audio', and 'Tools'. The 'Audio' tab is active, showing settings for 'PCM Sine Wave' and 'Compr. Audio'. The 'Channels' dropdown is set to '7.1', 'Sample Rate' is '48 kHz', and 'Bits/Sample' is '24'. A 'Channel Selection' row contains buttons for channels 1 through 8, with channel 1 highlighted. Below this, 'Channel: 1 Mute' is set to 'Off'. The 'Level (dB)' section has buttons for -3dB, -48, +3dB, and -1000, with -48 selected. The 'Frequency (Hz)' section has buttons for 1000 and +1000, with 1000 selected. At the bottom, there are 'APPLY', 'STATUS', and 'CLOSE' buttons.

HDMI Audio Generator – Compressed Formats

- ◆ HDMI Audio Generator:
 - ◆ Test UHD TVs and A/V receivers with a variety of audio formats.
 - ◆ Select from a variety of compressed audio clips.
 - ◆ Provides Dolby and DTS audio clips for replay.



HDMI 2.1 Sink Testing EDID and SCDC Testing

HDMI Video Generator – EDID Decode and Verification

- ◆ HDMI Video Generator:
 - ◆ Test 4K and 8K UHD TVs with a variety of video formats and colorimetry settings.
 - ◆ Verify EDID and SCDC register content of connected display.



Generator

MODES: FRL FRD:4/10G FMT:4320p60 F-Rate:1485.00MHz F-Rate:60.00Hz Output
INTF:HDMI DSC:No IMG:SmpteBar H-Rate:264.00kHz
(199) 7680x4320p @ 60 Hz 16:9 7680x4320 Progressive YCbCr-420: BT.2020-YCC-10bpc

Format Pattern Audio Tools

EDID Decode Read Save Load Edit

EDID Comp Block #01

HDCP CTA Data Block: Tag 3, bytes 24: Vendor Specific

SCDC Editor 24-bit IEEE Registration ID: 0x000C03
HDMI 1.4b Vendor Specific Data Block
CEC Physical Address: 1.0.0.0

Link Train ISRC/ACP: supported

DSC Deep Color
48 bits per color
36 bits per color
30 bits per color

AFC YCbCr 4:4:4 supported

InfoFrame DVI dual-link: Not supported
Max TMDS clock: 340 MHz

Image Ctrl Content types:
Game
Cinema
Photo
Graphics (text)

CEC Ping

CEC Tester

UHDA Test Latency: Not Present
Interlaced Latency: Not Present

HDR Lab Basic 3D: Supported
Image Size: Only indicates correct aspect ratio.

HDR10+ 4K x 2K Support:
3840x2160 30Hz
3840x2160 25Hz
3840x2160 24Hz
4096x2160 24Hz

Dolby Vision General 3D Support: On the SVDS listed below.
Frame packing
Top-and-Bottom
Side-by-Side (Half)
For SVDS:
002: (5) 1920x1080i @ 60 Hz 16:9
003: (32) 1920x1080n @ 24 Hz 16:9

Block 2/2 Page 4/13

DISCONNECT Refresh eARC Master TX 48G Generator HDMI CLOSE

HDMI Video Generator – EDID Decode with DSC

- ◆ HDMI Video Generator:
 - ◆ Test 4K and 8K UHD TVs with a variety of video formats and colorimetry settings.
 - ◆ Verify EDID and SCDC register content of connected display.
 - ◆ The example shows that the sink EDID is showing support for Display Stream Compression (DSC).



Generator

MODE:FRL FRL:4/12G FMT:4320p60 P-Rate:2376.00MHz F-Rate:60.00Hz Output
INTF:HDMI DSC:No IMG:SmpteBar 7680x4320 Progressive RGB-8bpc H-Rate:264.00kHz

(199) 7680x4320p @ 60 Hz 16:9

Format Pattern Audio Tools

EDID Decode Read Save Load Edit

EDID Comp Block #01

HDCP CTA Data Block: Tag 3, bytes 13: Vendor Specific
24-bit IEEE Registration ID: 0xC45DD8

SCDC Editor HDMI Forum Vendor Specific Data Block

Link Train
* Version: 1
* Max_TMDS_Character_Rate: 600 MHz
* Max_FRL_Rate: 12 Gbps @ 4 Lanes

DSC
Y: SCDC_Present
N: RR_Capable
N: CABLE_STATUS
N: CCBPCI

3D
Y: LTE_340MHz_scramble
N: Independent_view

AFC
N: Dual_View
N: 3D_OSD_Disparity

InfoFrame
N: UHD_VIC

Image Ctrl
Y: DC_48bit_420
Y: DC_36bit_420
Y: DC_30bit_420

CEC Ping
N: Mdelta

CEC Tester
N: CinemaVRR

UHDA Test
N: CNMVRR
N: EVA
N: ALLM
N: FAPA_start_location

HDR Lab
N: FAPA_start_location

HDR10+
* VRRmin: 0 Hz
* VRRMax: 0 Hz

Dolby Vision
Y: DSC_10bpc
Y: DSC_12bpc
Y: DSC_16bpc
Y: DSC_1p2
Y: DSC_All_bpp
Y: DSC_Native_420

Editors
* DSC_Max_FRL_Rate: 12 Gbps
* DSC_MaxSlices: Up to 16 slices and up to (400 MHz/KSliceAdjust) pixel clock per slice
* DSC_TotalChunkKBytes: 63 = 65536 bytes

Scripts

Block 2/2 Page 5/11

CLOSE



HDMI Video Generator – Compare EDIDs

- ◆ HDMI Video Generator:
 - ◆ View and verify EDID contents of a connected display. Check for checksum and header errors
 - ◆ Check EDID against known-reference or read the same EDID successively.
 - ◆ Report provides details difference.



MODE:FRL FRL:4/10G FMT:4320p60 F-Rate:1485.00MHz F-Rate:60.00Hz
Output

INTF:HDMI DSC:No IMG:SmpteBar
7680x4320 Progressive YCbCr-420: BT.2020-YCC-10bpc

(199) 7680x4320p @ 60 Hz 16:9
7680x4320 Progressive YCbCr-420: BT.2020-YCC-10bpc

Format
Pattern
Audio
Tools

Select the EDIDs to Compare

Edid #1 Read from Sink

Edid #2 1200MHz_10G

COMPARE

The EDIDs are different.

#1: Read from Sink #2: 1200MHz_10G

Block 2/2

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
00	02	03	59149	F0	59152	10	05	20	22	04	03	02	07	06	5D	5E
10	5F	60	61	62	64	65	66	C2123	C410F	C317E	76107	75178	7E103	7D10C	23100	0F110
20	7F100	071F8	78	0312F	0C1C8	0015A	10101	00102	F9103	44104	2F181	C9141	8A100	01116	02106	03108
30	04100	81156	41158	00	16167	061D8	0815D	001C4	5E101	59178	00188	67157	D91E2	5D100	C4148	01183
40	7917F	88100	67100	E21E1	0010F	4B1E3	83106	7F107	00101	00101	E111D	0F180	E4118	0E171	C711C	C6116
50	C5120	E3158	0612C	0F125	01100	E31BA	05188	FF121	01100	5E100	5E19E	00156	A015E	A0100	A0	291A0
60	501A0	30129	20150	35130	00120	BA135	88100	211BA	00188	00121	1A100	66100	2111A	5E166	AA121	51156
70	001AA	1E151	30100	4611E	8F130	33146	0018F	BA133	88100	211BA	00188	00121	1E100	00	0011E	DD110

DECODE AND DIFF

Video Generator – Verify SCDC Registers

- ◆ HDMI Video Generator:
 - ◆ Read and verify HDMI SCDC register values for capabilities, configuration and status.



The screenshot shows the 'Generator' software interface. The 'SCDC Editor' menu item is highlighted in the left sidebar. The main window displays the 'Status Flags' register values for the SCDC Editor. The register values are as follows:

Bit	Value	Description
Bit 3	0 1	Rsvd (0)
Bit 4	0 1	Rsvd (0)
Bit 5	0 1	Rsvd (0)
Bit 6	0 1	Rsvd (0)
Bit 7	0 1	Rsvd (0)

Below the Status Flags, the '0x40 (R) Status_0' register is shown with the following bit values:

Bit	Value	Description
Bit 0	0 1	Clock Detected
Bit 1	0 1	Ch0_Ln0_Locked
Bit 2	0 1	Ch1_Ln1_Locked
Bit 3	0 1	Ch2_Ln2_Locked
Bit 4	0 1	Lane3_Locked
Bit 5	0 1	Reserved
Bit 6	0 1	FLT_Ready
Bit 7	0 1	DSC_DecodeFail

The '0x41 (R) Status_1' register is also shown with dropdown menus for 'Bits 0-3: Ln0_LTP_req' and 'Bits 4-7: Ln1_LTP_req', both set to '0: No Pattern Requested'.

HDMI 2.1 Sink Testing Compliance Testing

HDMI Fixed Rate Link (FRL) Sink Compliance Test

◆ HDMI 2.1 FRL sink compliance Testing:

- ◆ Run FRL sink compliance tests.
Full list of tests supported (partial list shown right).



The screenshot displays the 'FRL Sink' test interface. At the top, it shows the instrument 'ALM41d [10.30.196.30]' and a 'Connect' button. Below this is a table with columns for 'CDF Entry', 'Test Selection', and 'Test Options / Preview'. A 'Select All' button with a green checkmark and a red 'x' is visible. A green 'EXECUTE TESTS' button is in the top right corner. The main area lists various tests, each with a green checkmark in the right margin, indicating they are passed. The tests are grouped into categories: CED, RS, 8bpc Decoding, DC Decoding, 8bpc Timing, and DC Timing. At the bottom, there is a 'CLOSE' button and a partially visible test entry for 'HFR2-30: Audio Decoding and Rendering (FRL Mode) - MS Audio (L-PCM and 61937) - Sample Packet'.

CDF Entry	Test Selection	Test Options / Preview
Select All ✓ ✗ EXECUTE TESTS		
▼ CED		
>	HFR2-17: Sink FRL Protocol - CED - Lock Bits	✓
>	HFR2-18: Sink FRL Protocol - CED - Error Counting During Reads	✓
>	HFR2-19: Sink FRL Protocol - CED - Specific Video Data Error Injection	✓
>	HFR2-20: Sink FRL Protocol - CED - Maximum Video Data Error Injection	✓
>	HFR2-21: Sink FRL Protocol - CED - Update Flag with Specific Error Injection	✓
>	HFR2-22: Sink FRL Protocol - CED - Update Flag with Maximum Error Injection	✓
▼ RS		
>	HFR2-48: Sink FRL Protocol - RS - Basic Operation	✓
>	HFR2-49: Sink FRL Protocol - RS - Correction Counting During Reads	✓
>	HFR2-50: Sink FRL Protocol - RS - Maximum Symbol Error Count	✓
>	HFR2-51: Sink FRL Protocol - RS - Update Flag with Specific Symbol Error Count	✓
>	HFR2-52: Sink FRL Protocol - RS - Update Flag with Maximum Symbol Error Count	✓
▼ 8bpc Decoding		
>	HFR2-23: Sink Pixel Decoding (FRL Mode) - YCbCr 4:2:0	✓
>	HFR2-31: Sink Pixel Decoding (FRL Mode) - RGB	✓
>	HFR2-32: Sink Pixel Decoding (FRL Mode) - YCbCr 4:2:2/4:4	✓
▼ DC Decoding		
>	HFR2-24: Pixel Decoding (FRL Mode) - YCbCr 4:2:0 Deep Color	✓
>	HFR2-33: Sink Pixel Decoding (FRL Mode) - Non-YCbCr 4:2:0 Deep Color	✓
▼ 8bpc Timing		
>	HFR2-11: Sink Video Timing (FRL Mode) - Sub-2160p 24-bit Color Depth	✓
>	HFR2-12: Sink Video Timing (FRL Mode) - 2160p 24-bit Color Depth	✓
>	HFR2-13: Sink Video Timing (FRL Mode) - 4320p 24-bit Color Depth	✓
▼ DC Timing		
>	HFR2-14: Sink Video Timing (FRL Mode) - Sub-2160p Deep Color	✓
>	HFR2-15: Sink Video Timing (FRL Mode) - 2160p Deep Color	✓
HFR2-30: Audio Decoding and Rendering (FRL Mode) - MS Audio (L-PCM and 61937) - Sample Packet		
CLOSE		

HDMI Fixed Rate Link (FRL) Sink Compliance Test

◆ HDMI 2.1 FRL sink compliance Testing:

- ◆ Run FRL sink compliance tests. Full list of tests supported.
- ◆ Provides detailed Test Results with Pass/Fail and details for each subtest.
- ◆ Enables compliance self-testing and/or pre-testing of FRL devices.
- ◆ Enables export of compliance test results to share w/ colleagues.

The screenshot shows the 'Compliance Test Results Viewer' window. The title bar reads 'FRL Sink (2.1b) Compliance Test Results'. The main area displays test results for 'AA_NVK_RS_48_Full' with a date of 'December 11, 2018 11:14 AM' and manufacturer 'gd'. The overall status is 'CIS 2.1b - Fail'. A table lists test results with columns for 'Test Name / Details' and 'Status'. A yellow arrow points to a failed test step: 'Sink RS_C_Valid flags not 0 80'. Below the table, the instrument ID '55980B [10.30.196.240]' is visible.

Test Name / Details	Status
HFR2-48: Sink FRL Protocol - RS - Basic Operation	Pass
Iter 01: 3 Lanes	Pass
Iter 02: 4 Lanes	Pass
01: 1. CDF field Source Max FRL Rate is 0 then skip the test.	Pass
02: 4. Read the RSCC, verify that RS C Valid flag = 0; otherwise FAIL.	Fail
0xA8:59/5A 0:80	
Sink RS_C_Valid flags not 0 80	
0xA8:59/5A 0:80	
Sink RS_C_Valid flags not 0 80	
03: 7. Read each FRL Lock bit. Repeat until all FRL Lock bits are set (=1) on all ac	Pass
04: 8. Read the FRL Start flag. Repeat until FRL Start is set (=1), else FAIL after	Pass
05: 10. Read the RSCC, verify that RS C Valid flag = 1 and count = 0 or 1; otherwise	Pass
06: 11. Corrupt symbols at a rate of about 1e-9, spaced out over 10 seconds, with 1	Pass
07: 12. Read the RSCC; if the value is not correct within 1 count then FAIL.	Pass
08: 13. Read the RSCC again after 100 milliseconds; if the count is not 0 or 1 then	Pass
09: 14. Corrupt symbols at a rate of about 2e-9, spaced out over 10 seconds, with 2	Pass
10: 15. Read the RSCC; if the value is not correct within 1 count then FAIL.	Pass
11: 16. Corrupt one symbol in each of 4 consecutive RS blocks, after generating the	Pass
12: 17. Change the FRL data stream to be random data on all lanes.	Pass
13: 18. After 5 seconds, read each FRL Lock bit and verify that they have all been c	Pass
14: 19. Read the RSCC, verify that RS C Valid flag = 1; otherwise FAIL	Pass
15: 20. If the count in the RSCC is less than 4, then FAIL.	Pass
HFR2-49: Sink FRL Protocol - RS - Correction Counting During Reads	Fail
Iter 01:	Fail
01: 1. CDF field Source Max FRL Rate is 0 then skip the test.	Pass
02: 2. Perform Link Training at the minimum FRL Rate with the maximum number of FRL	Pass
03: 4. Read each FRL Lock bit. Repeat until all FRL Lock bits are set (=1) on all ac	Pass
04: 7. Read the RSCC, verify that RS C Valid flag = 1 and count = 0 or 1; otherwise F	Pass
05: 8. Corrupt one symbol in each of a known random number (between 10000 and 30000)	Pass
06: 9. 100 milliseconds after the start of the symbol error, read the RSCC and add t	Pass
07: 11.1. If the correction count is outside the range of ±2 from the number of gene	Fail
HFR2-50: Sink FRL Protocol - RS - Maximum Symbol Error Count	Pass
HFR2-51: Sink FRL Protocol - RS - Update Flag with Specific Symbol Error Count	Pass
HFR2-52: Sink FRL Protocol - RS - Update Flag with Maximum Symbol Error Count	Pass

HDMI TMDS Sink Compliance Test

◆ HDMI TMDS compliance Testing:

- ◆ Run TMDS sink compliance tests. Full list of tests supported (partial list shown right).

Test Name	Status
TMDS Protocol	
> HF2-5: TMDS Protocol - 6G - Scrambling	✓
> HF2-9: TMDS Protocol - Scrambling <= 340Mcsc	✓
Pixel Decoding	
> HF2-23: Pixel Decoding - YCBCR 4:2:0	✓
> HF2-24: Pixel Decoding - YCBCR 4:2:0 Deep Color	✓
> HF2-71: Pixel Decoding - YCBCR 4:2:0 for 861G Video Formats	✓
> HF2-72: Pixel Decoding - YCBCR 4:2:0 Deep Color for 861G Video Formats	✓
EDID	
> HF2-10: Video Timing - 6G - HF-VSDB	✓
> HF2-26: EDID - Video Format Declaration	✓
> HF2-31: EDID - YCBCR 4:2:0 - Data Blocks	✓
> HF2-32: EDID - YCBCR 4:2:0 BT.2020 - Data Block	✓
> HF2-35: EDID YCBCR 4:2:0 Deep Color HF-VSDB	✓
> HF2-39: EDID 3D and Multi-stream Audio Data Blocks	✓
> HF2-41: HDMI VSDBs - Independent-View	✓
> HF2-53: EDID - HF-VSDB	✓
> HFR2-53: Sink Video Timing - FRL/Gaming/DSC - HF-VSDB	✓
> HFR2-70: Sink EDID - HF-VSDB Reserved Bits	✓
Timing 6G	
> HF2-6: Video Timing - 6G - 2160p 24-bit Color Depth	✓
> HF2-7: Video Timing - 6G - Deep Color	✓
> HF2-8: Video Timing - 6G - 2160p 3D	✓
Timing 21:9	
> HF2-25: Video Timing - 21:9 (64:27)	✓
HDMI-VSIFs	
> HF2-40: HDMI VSIFs - Dual-View	✓

HDMI TMDS Sink Compliance Test

- ◆ HDMI TMDS compliance Testing:
 - ◆ Run TMDS sink compliance tests. Full list of tests supported.
 - ◆ Provides detailed Test Results with Pass/Fail and details for each subtest.
 - ◆ Enables compliance self-testing and/or pre-testing of HDMI TMDS devices.
 - ◆ Enables export of compliance test results to share with colleagues.

The screenshot displays the 'Compliance Test Results Viewer' window. The title bar reads 'HDMI 2.0 Sink (2.0) Compliance Test Results'. The main area shows test details for 'Test_ID_2-5_1' performed on 'May 22, 2014 10:45 AM' by 'Manufacturer: ACME' and 'Model Name: XYZ'. The 'Overall Status' is 'CTS 2.0 - Pass' and 'Port Tested: 1'. A table lists test results, with 'HF2-5: TMDS Protocol - 6G - Scrambling' and its subtest 'Iter 01' both marked as 'Pass'. The 'Iter 01' subtest includes details: 'Test Format: (97) 3840x2160p @ 60 Hz 16:9, 24 bpp', 'Scrambling_Status bit was set to 1.', and 'Manual inspection of the DUT verified adequate support of the'. At the bottom, the 'Instrument' is '980B_MKC [192.168.254.161]' and there are buttons for 'Continue Test Execution' and 'Close'.

Test Name / Details	Status
HF2-5: TMDS Protocol - 6G - Scrambling	Pass
Iter 01:	Pass
• Test Format: (97) 3840x2160p @ 60 Hz 16:9, 24 bpp	
• Scrambling_Status bit was set to 1.	
• Manual inspection of the DUT verified adequate support of the	

HDMI TMDS Sink Compliance Test

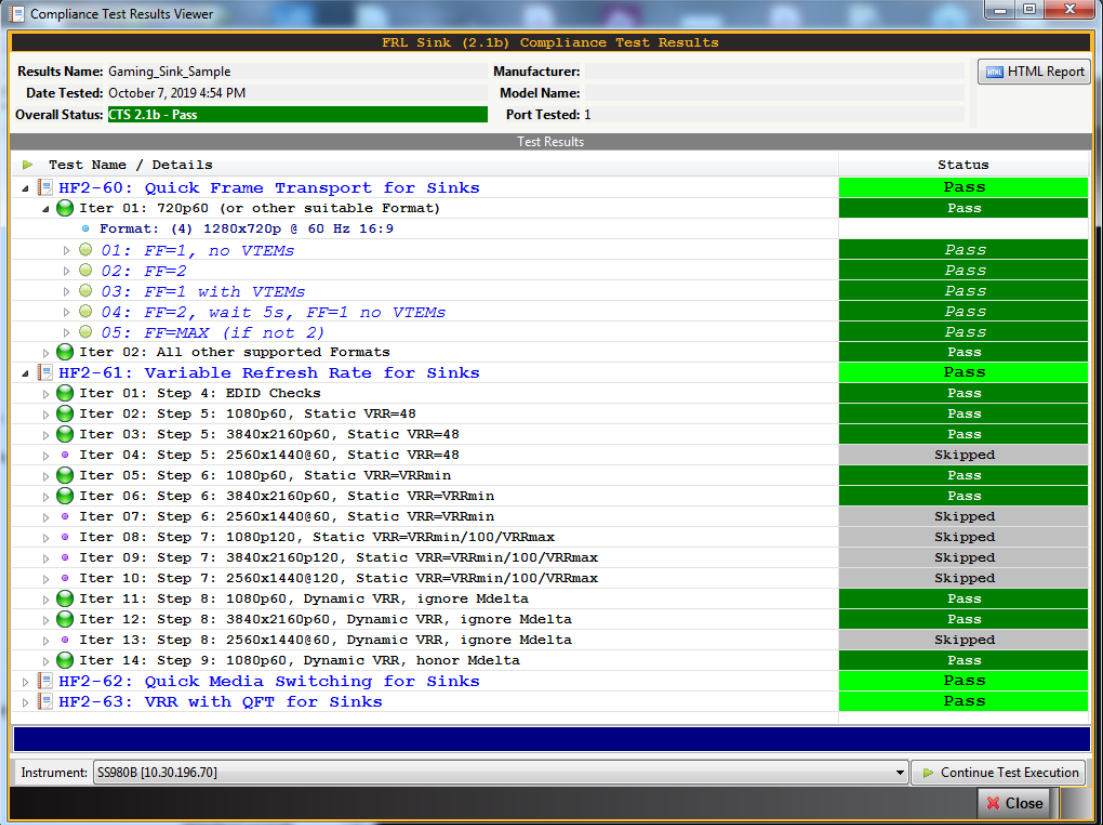
- ◆ HDMI TMDS compliance Testing:
 - ◆ Run TMDS sink compliance tests. Full list of tests supported.
 - ◆ Provides detailed Test Results with Pass/Fail and details for each subtest.
 - ◆ Enables compliance self-testing and/or pre-testing of HDMI TMDS devices.
 - ◆ Enables export of compliance test results to share with colleagues.

The screenshot displays the 'Compliance Test Results Viewer' window. The title bar reads 'HDMI 2.0 Sink (2.0) Compliance Test Results'. The main area shows test details: Results Name: Test_ID_2-9_1, Date Tested: May 22, 2014 12:08 PM, Overall Status: **CTS 2.0 - Pass**, Manufacturer: ACME, Model Name: XYZ, and Port Tested: 1. A table titled 'Test Results' lists the test 'HF2-9: TMDS Protocol - Scrambling <= 340Msc' with a status of 'Pass'. It includes subtests for 'Iter 01:' and '01: (2) 720x480p @ 60 Hz 4:3, Not Scrambled', both with 'Pass' status. At the bottom, the instrument is identified as '980B_MKC [192.168.254.161]' and there are buttons for 'Continue Test Execution' and 'Close'.

Test Name / Details	Status
HF2-9: TMDS Protocol - Scrambling <= 340Msc	Pass
Iter 01:	Pass
01: (2) 720x480p @ 60 Hz 4:3, Not Scrambled	Pass

HDMI FRL/TMDS Gaming Sink Compliance Test

- ◆ HDMI 2.1 FRL/TMDS Gaming sink compliance Testing:
 - ◆ Run FRL/TMDS Gaming sink compliance tests:
 - ◆ Quick Frame Transport (QFT).
 - ◆ Variable Refresh Rate (VRR).
 - ◆ Quick Media Switching (QMS).
 - ◆ VRR with QFT.
 - ◆ ALLM (not currently supported).
 - ◆ Provides detailed Test Results with Pass/Fail and details for each subtest.
 - ◆ Enables compliance self-testing and/or pre-testing of FRL or TMDS Gaming-capable devices.
 - ◆ Enables export of compliance test results to share w/ colleagues.



Compliance Test Results Viewer

FRL Sink (2.1b) Compliance Test Results

Results Name: Gaming_Sink_Sample Manufacturer: HTML Report

Date Tested: October 7, 2019 4:54 PM Model Name: Port Tested: 1

Overall Status: **CTS 2.1b - Pass**

Test Results

Test Name / Details	Status
▶ HF2-60: Quick Frame Transport for Sinks	Pass
▶ Iter 01: 720p60 (or other suitable Format)	Pass
▶ Format: (4) 1280x720p @ 60 Hz 16:9	
▶ 01: FF=1, no VTEMS	Pass
▶ 02: FF=2	Pass
▶ 03: FF=1 with VTEMS	Pass
▶ 04: FF=2, wait 5s, FF=1 no VTEMS	Pass
▶ 05: FF=MAX (if not 2)	Pass
▶ Iter 02: All other supported Formats	Pass
▶ HF2-61: Variable Refresh Rate for Sinks	Pass
▶ Iter 01: Step 4: EDID Checks	Pass
▶ Iter 02: Step 5: 1080p60, Static VRR=48	Pass
▶ Iter 03: Step 5: 3840x2160p60, Static VRR=48	Pass
▶ Iter 04: Step 5: 2560x1440@60, Static VRR=48	Skipped
▶ Iter 05: Step 6: 1080p60, Static VRR=VRRmin	Pass
▶ Iter 06: Step 6: 3840x2160p60, Static VRR=VRRmin	Pass
▶ Iter 07: Step 6: 2560x1440@60, Static VRR=VRRmin	Skipped
▶ Iter 08: Step 7: 1080p120, Static VRR=VRRmin/100/VRRmax	Skipped
▶ Iter 09: Step 7: 3840x2160p120, Static VRR=VRRmin/100/VRRmax	Skipped
▶ Iter 10: Step 7: 2560x1440@120, Static VRR=VRRmin/100/VRRmax	Skipped
▶ Iter 11: Step 8: 1080p60, Dynamic VRR, ignore Mdelta	Pass
▶ Iter 12: Step 8: 3840x2160p60, Dynamic VRR, ignore Mdelta	Pass
▶ Iter 13: Step 8: 2560x1440@60, Dynamic VRR, ignore Mdelta	Skipped
▶ Iter 14: Step 9: 1080p60, Dynamic VRR, honor Mdelta	Pass
▶ HF2-62: Quick Media Switching for Sinks	Pass
▶ HF2-63: VRR with QFT for Sinks	Pass

Instrument: SS980B [10.30.196.70] Continue Test Execution

Close

HDMI Compliance Testing – Export Compliance Test Results

◆ HDMI Aux Compliance Test Results Export:

- ◆ Save compliance test results and HTML file for easy and universal viewing through browser.

HTML Viewer
C:\Users\inkendall\Documents\Current_Work\Marketing\PSG_WW_Sales\April_2018\QD_Resources\980_Practice_Utility\980mgr\fr\sinkct\results\My_FRL_Sink_CT_Test_1\Report_Cdf.htm

April 12, 2019 11:24 AM www.quantumdata.com

HDMI FRL Sink Compliance Test Report CTS 2.1b

Results Name:	My_FRL_Sink_CT_Test_1	Manufacturer:	ACME
Date Tested:	April 11, 2019 1:57 PM	Model Name:	XYZ
Overall Status:	Incomplete	Port Tested:	1

Capabilities Declaration Form (CDF)

FRL	
Sink_Max_FRL_Rate	12 Gbps @ 4 Lanes
Sink_Supports_ALLM	NO
Sink_Supports_VRR	NO
Sink_Supports_DSC	NO
Features	
Sink_Supports_4K100A	NO
Sink_Supports_4K100B	NO
Sink_Supports_4K120A	NO
Sink_Supports_4K120B	NO
Sink_Supports_8K50A	NO
Sink_Supports_8K50B	NO
Sink_Supports_8K60A	NO
Sink_Supports_8K60B	NO
DSC	
Sink_Supports_DSC	NO
6G - Video	

← Back → Forward Save As Close

HDMI Compliance Testing – Export Compliance Test Results

◆ HDMI Aux Compliance Test Results Export:

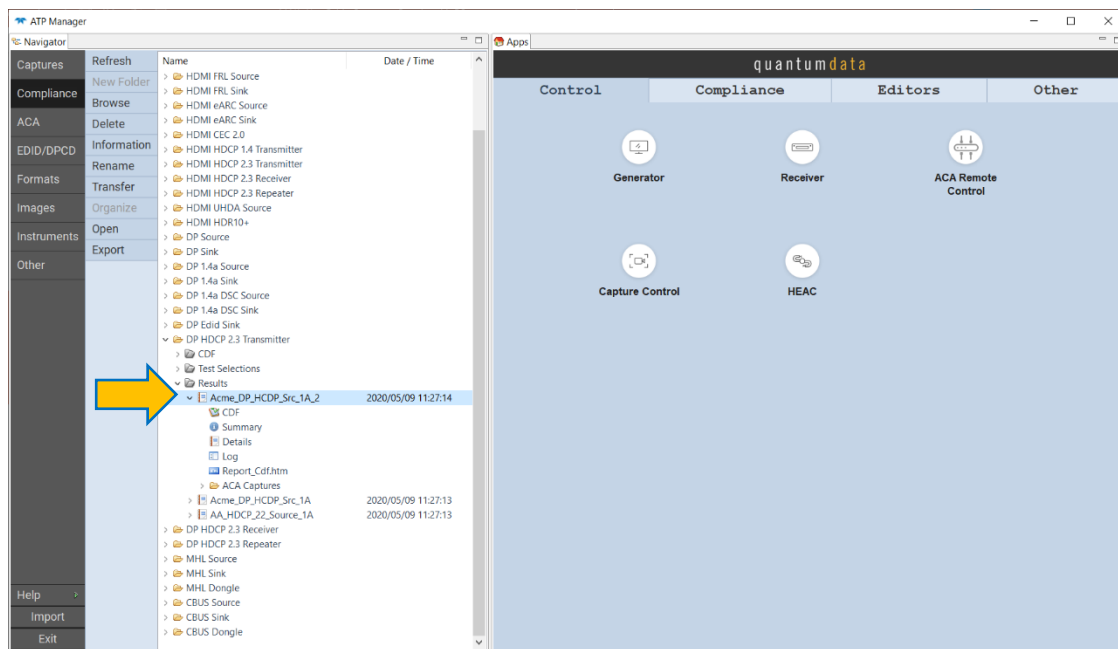
- ◆ Save compliance test results and HTML file for easy and universal viewing through browser.

Test HFR2-17 Sink FRL Protocol - CED - Lock Bits	Incomplete	
• Iter 01: 3 Lanes	User Skipped	
• Iter 02: 4 Lanes	Pass	
• 01: 1. CDF field Source_Max_FRL_Rate is 0 then skip the test.		Pass
• Cable Connected. link trained for 4 lanes 3 rate.		
• 02: 3. Read the EDID after HPD is asserted.		Pass
• 03: 4. Read each FRL Lock bit. If any FRL Lock bits are set (=1), then FAIL.		Pass
• 04: 7. Read each FRL Lock bit after 10 milliseconds. If any FRL Lock bits are cleared (=0) on any active Lanes, then FAIL.		Pass
• 4 lanes, testing lane(0xF=all):0xf, FRL LOCK bits:0x5e exp:0xf mask:0xf		
• 05: 8. Read the FRL_Start flag after 200 milliseconds. If FRL_Start is not set (=1), then FAIL		Pass
• 06: 11. Read the FRL Lock bit for Lane 0 after 10 milliseconds, verify that the bit is still set (=1). If the FRL Lock bit has cleared (=0), then FAIL		Pass
• 4 lanes, testing lane(0xF=all):0x0, FRL LOCK bits:0x5e exp:0x1 mask:0x1		
• 4 lanes, testing lane(0xF=all):0x1, FRL LOCK bits:0x5e exp:0x2 mask:0x2		
• 4 lanes, testing lane(0xF=all):0x2, FRL LOCK bits:0x5e exp:0x4 mask:0x4		
• 4 lanes, testing lane(0xF=all):0x3, FRL LOCK bits:0x5e exp:0x8 mask:0x8		
• 07: 13. After at least 2 Super Blocks, read Lane 0 Lock bit and verify it has been cleared (=0). If the FRL Lock bit is set (=1), then FAIL.	Pass	
• 4 lanes, testing lane(0xF=all):0x0, FRL LOCK bits:0x5c exp:0x0 mask:0x1		
• 4 lanes, testing lane(0xF=all):0x1, FRL LOCK bits:0x5a exp:0x0 mask:0x2		
• 4 lanes, testing lane(0xF=all):0x2, FRL LOCK bits:0x56 exp:0x0 mask:0x4		
• 4 lanes, testing lane(0xF=all):0x3, FRL LOCK bits:0x4e exp:0x0 mask:0x8		

HDMI Compliance Testing – Export Compliance Test Results

◆ HDMI Aux Compliance Test Results Export:

- ◆ Save compliance test results and HTML file for easy and universal viewing through browser.
- ◆ Export compliance test results for dissemination to colleagues, other subject matter experts or Teledyne Customer Support.



HDMI 2.1 Sink Testing

HDCP Compliance Testing

HDMI HDCP 2.3 Sink Compliance Testing

- ◆ HDMI HDCP 2.3 compliance Testing:
 - ◆ Run HDCP 2.3 sink compliance tests. All tests supported.
 - ◆ Provides detailed Test Results with Pass/Fail and details for each subtest.
 - ◆ Enables compliance self-testing and/or pre-testing of HDMI devices.
 - ◆ Enables export compliance test results to share with colleagues.

Compliance Test Results Viewer

DP HDCP 2.2 Receiver (1.0) Compliance Test Results

Results Name: AA_Com_Monitor_1 Manufacturer: LG
Date Tested: March 15, 2017 7:57 PM Model Name: 5K Monitor
Overall Status: **CTS 1.0 - Pass** Port Tested: 1

HTML Report

Test Name / Details	Status
2C-01: Regular Procedure - With transmitter	Pass
Iter 01: With previously not connected receiver	Pass
Iter 02: With previously connected receiver	Pass
TX:HPD::ENTER	
TX HPD:**Test Cond.** auth	
TX UNAUTH::ENTER	
TX MSGR:Disable ENC_EN ts:3957204961.28 us	
TX UNAUTH:AKE_INIT ts:3958706882.56 us	
TX UNAUTH:MSG RD:AKE_Init ts:3958706882.56 us	
TX UNAUTH:MSG RCVD:AKE_Send_Cert ts:3958759403.52 us	
TX UNAUTH:Rrx 0,7f,d4,f0,cf,b3,4c,86	
TX UNAUTH:RxCaps 2 0 2	
TX AKE:Snd Stored_RM ts:3958786918.40 us	
TX AKE:MSG:AKE_Storage ts:3958786918.40 us	
TX AKE:MSG RCVD:AKE_Send_H_prime ts:3958822830.08 us	
TX LC:Snd LC_Init ts:3958824253.44 us	
TX LC:MSG:LC_Init ts:3958824253.44 us	
TX LC:MSG RCVD:LC_Send_L_prime ts:3958831534.08 us	
TX SKE:Snd SKE_Send_EKS ts:3958833356.80 us	
TX:AUTH::ENTER	
TX AUTH:Snd STRM_TYPE ts:3958843596.80 us 0	
TX MSGR:Enable ENC_EN ts:3959084165.12 us	
TX AUTH:MSG:SKE_Send_Eks ts:0.00 us	
Transmitted test pattern was visible on the Sink DUT.	
2C-02: Irregular Procedure - New Authentication after AKE Init	Pass
2C-03: Irregular Procedure - New Authentication during Locality Check	Pass
2C-04: Irregular Procedure - New Authentication after SKE Send Eks	Pass
2C-05: Irregular Procedure - New Authentication during Link Synchronization	Pass
2C-06: Regular Procedure - Encryption Disable Bootstrapping	Pass

Instrument: S9980B [10.30.196.70] Continue Test Execution

Close

HDMI HDCP 2.3 Sink Compliance Testing

- ◆ HDMI HDCP 2.3 compliance Testing:
 - ◆ Run HDCP 2.3 sink compliance tests. All tests supported.
 - ◆ Provides detailed Test Results with Pass/Fail and details for each subtest.
 - ◆ Enables compliance self-testing and/or pre-testing of HDMI devices.
 - ◆ Enables export compliance test results to share with colleagues.

Compliance Test Results Viewer

HDMI HDCP 2.3 TX (1.0) Compliance Test Results

Results Name: AA_HDMI_HDCP_22_PC Manufacturer: Nvidia
Date Tested: May 17, 2016 3:57 PM Model Name: GTX
Overall Status: **CTS 1.0 - Fail** Port Tested: 1

HTML Report

Test Name / Details	Status
1A-01: Regular Procedure: With previously connected Receiver (With stored Km)	Pass
Iter 01:	Pass
1A-02: Regular Procedure: With newly connected Receiver (Without stored Km)	Pass
1A-03: Regular Procedure: Receiver disconnect after AKE Init	Pass
1A-04: Regular Procedure: Receiver disconnect after Km	Pass
1A-05: Regular Procedure: Receiver disconnect after locality check	Pass
1A-06: Regular Procedure: Receiver disconnect after Ks	Fail
Iter 01:	Fail
Clear Ready	
RX HPD Deasserted regular ts:5115282636.80 us	
RX HPD Asserted regular ts:5115432673.28 us	
RX UNAUTH::ENTER	
RX UNAUTH:HDMI/VIDEO Present	
RX UNAUTH:MSG RD:ENC_DIS ts:5115992064.00 us	
RX UNAUTH:RCVD:AKE_Init ts:0.00 us	
RX UNAUTH:**Test Cond.** hpd	
RX AKE:MSG SND:AKE_Send_Cert ts:5117223004.16 us	
RX AKE:MSG RCVD:AKE_No_Stored_km ts:5118022901.76 us	
RX PAIR::ENTER	
RX PAIR:MSG RD:AKE_Send_H_Prime ts:5118037442.56 us	
RX LC:MSG SND:AKE_Send_Pairing_Info ts:5118050856.96 us	
RX LC:MSG RCVD:LC_Init ts:5118052044.80 us	
RX LC:MSG SND:LC_Send_L_prime ts:5118058301.44 us	
RX LC:MSG RCVD:SKE_Send_Eks ts:5118072350.72 us	
RX SKE::ENTER	
RX SKE:MSG RCVD:SKE_Send_Eks ts:5118072350.72 us	
RX HPD Deasserted irregular ts:5118072606.72 us	
RX HPD Asserted irregular ts:5118272634.88 us	
RX UNAUTH:MSG RD:ENC_EN ts:5118292039.68 us	
Encryption Enabled	
1A-07: Regular Procedure: Receiver sends REAUTH REQ after Ks	Pass
1A-08: Irregular Procedure: Rx certificate not received.	Pass

Instrument: SS980B [10.30.196.70] Continue Test Execution

Close

HDMI HDCP 2.3 Sink Compliance Test - ACA Test Capture Logs

HDMI Aux Channel Analyzer Timestamp control:

- ◆ View the ACA transaction files for each HDCP test to confirm failures.
- ◆ View details of any transaction.
- ◆ View time stamps.

The screenshot shows the ACA Data Viewer interface with a list of HDCP transactions on the left and a detailed view of a selected transaction on the right.

Time	Event	Source	Destination	Rate	Details
813	HDCP	HDMI2-R60	< 0000	(87.77 kbps)	
814	EDID	HDMI2-R60	R EDID 00	(87.61 kbps)	
815	EDID	HDMI2-R60	< 128 bytes	(87.61 kbps)	
816	EDID	HDMI2-R60	R EDID 80	(87.61 kbps)	
817	EDID	HDMI2-R60	< 128 bytes	(87.61 kbps)	
818	SCDC	HDMI2-R60	W TMD5_Config 00	(86.54 kbps)	
820	EDID	HDMI2-R60	W Segment 00	(87.77 kbps)	
821	HDCP	HDMI2-R60	R HDCP2Version	(87.61 kbps)	
822	HDCP	HDMI2-R60	< 04	(87.77 kbps)	
823	HDCP	HDMI2-R60	W AKE_Init	(87.77 kbps)	
824	HDCP	HDMI2-R60	R RxStatus	(87.77 kbps)	
825	HDCP	HDMI2-R60	< 1602	(87.77 kbps)	
826	HDCP	HDMI2-R60	R Read_Message	(87.77 kbps)	
827	HDCP	HDMI2-R60	< AKE_Send_Cert	(87.77 kbps)	
828	HDCP	HDMI2-R60	R RxStatus	(87.77 kbps)	
829	HDCP	HDMI2-R60	< 0000	(87.77 kbps)	
830	HDCP	HDMI2-R60	R RxStatus	(87.77 kbps)	
831	HDCP	HDMI2-R60	< 0000	(87.77 kbps)	
832	HDCP	HDMI2-R60	R RxStatus	(87.77 kbps)	
833	HDCP	HDMI2-R60	< 0000	(87.77 kbps)	
834	HDCP	HDMI2-R60	R RxStatus	(87.77 kbps)	
835	HDCP	HDMI2-R60	< 0000	(87.77 kbps)	
836	HDCP	HDMI2-R60	W AKE_Stored_km	(87.77 kbps)	
837	HDCP	HDMI2-R60	R RxStatus	(87.77 kbps)	
838	HDCP	HDMI2-R60	< 2100	(87.77 kbps)	
839	HDCP	HDMI2-R60	R Read_Message	(87.77 kbps)	
840	HDCP	HDMI2-R60	< AKE_Send_H_prime	(87.77 kbps)	
841	HDCP	HDMI2-R60	W LC_Init	(87.77 kbps)	
842	HDCP	HDMI2-R60	R RxStatus	(87.77 kbps)	
843	HDCP	HDMI2-R60	< 2100	(87.77 kbps)	
844	HDCP	HDMI2-R60	R Read_Message	(87.77 kbps)	
845	HDCP	HDMI2-R60	< LC_Send_L_prime	(87.77 kbps)	
846	HDCP	HDMI2-R60	W SKE_Send_Eks	(87.77 kbps)	
847	HDCP	HDMI2-R60	R RxStatus	(87.77 kbps)	

The detailed view on the right shows the following information for the selected transaction:

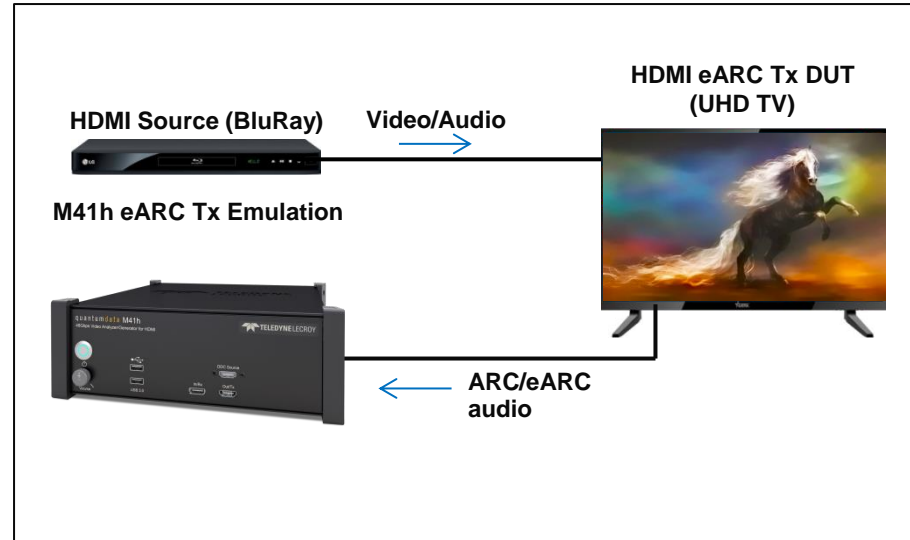
- Type: HDCP
- Start Time: +00:15:46.907842
- Duration: 54.067 msec
- Maximum I2C Rate: 87.77 kbps
- Read: 534 bytes
- Register: 80h
- Name: Read_Message
- Message: AKE_Send_Cert (534 bytes)
- msg_id: 3
- cert_rx: [4175..0]
- Receiver ID: 8C 23 BA D5 A6
- Receiver Public Key:
 - C5 3B FC EC 4E 2A 42 EA 71 76 FA B8 90 7A EC 7B
 - F5 78 07 11 97 35 CE D6 F8 09 30 D3 DB AC 91 C4
 - 7D 82 CE F6 7D 7F 22 1A 1D A7 9F 6F C1 4A 52 16
 - AE 09 5A CC 59 FD 5F C2 07 19 D8 A7 02 D0 4C 85
 - B8 16 74 DA 3A 12 8B 00 84 E1 D3 2E 2C EA 76 05
 - 83 F8 12 B0 74 E6 B9 CB 5B BD BB FB 39 A3 26 4A
 - DF B9 E9 5A BD 0F 97 89 73 63 38 2B 95 1D 52 84
 - CA 1F 07 46 F1 14 36 1A 3F 61 BE 2E C2 E2 75 B3
 - 01 00 01
- RESERVED: 00 00
- DCCP LLC Signature:
 - 28 A8 50 53 80 72 16 76 A3 EB 07 D7 FC F7 A7 DB
 - 38 72 33 D5 26 76 87 64 3A D1 A4 45 45 86 6D 86
 - 9D 58 B4 3E 16 CD F8 E7 24 D7 74 F9 4E 76 C5 10
 - 1B D0 E8 4B 53 33 1A 6D 72 E2 3A 8A 79 FE BC CF
 - 52 9C 21 8E 4D 9F 8A 33 2E BA BF B4 69 36 C4 F0
 - DF BC 47 6B 5D 3B 4D 72 62 F3 19 82 24 85 EE 61
 - 4A DF 57 82 1F 03 23 DB DA 41 0B 25 79 28 FE A6
 - 72 ED 4D 42 1F D8 7F 31 A4 9A 97 97 8E 13 10 A5
 - 00 00 EB 48 97 71 5E 5C B5 1A 81 86 60 DB A9
 - CC 9A 2C 40 B8 1B 59 50 7B 2A 0B 46 EF DE CB 92
 - FF 8E AD E7 9A 0E FC D2 D2 1C 9E 35 25 2E C2 22
 - F7 CC 4C FE B2 0E C2 56 46 57 9F F5 1A 1A 32 FC
 - 5E E1 58 12 57 48 47 33 96 4C 0B 99 E7 C3 5E 6C
 - 61 E0 DD 86 23 BE 3E 97 82 4F 11 B4 70 86 2F 86
 - A8 C2 95 C1 F5 EC 39 8F 8C E3 7E FD 01 36 EE 0A
 - B2 F0 95 01 A4 74 92 F5 3C 10 9B 5B B9 60 61 FC
 - BC 6E 0C 07 DA 72 C7 74 B6 15 75 B1 65 A7 BF F3

HDMI 2.1 eARC Testing

Enhanced Audio Return Channel

HDMI eARC Tx Testing

- ◆ HDMI 2.1 eARC Testing:
 - ◆ Verify eARC Tx (TV) for common mode and differential mode operation.
 - ◆ Run eARC common and differential mode compliance tests for Tx devices. Full list of tests supported.



HDMI eARC Tx Testing

- ◆ HDMI 2.1 eARC Testing:
 - ◆ Verify eARC Tx (TV) for common mode and differential mode operation.
 - ◆ Run eARC common and differential mode compliance tests for Tx devices. Full list of tests supported (only partial list shown right).

The screenshot displays the 'eARC Source CT 1.0' application window. At the top, it shows 'Instrument: AL_M41d [10.30.196.30]' and 'Connect Cards'. Below this is a navigation bar with 'CDF Entry', 'Test Selection', and 'Test Options / Preview'. A 'Select All' button is on the left, and an 'EXECUTE TESTS' button is on the right. The main area contains a tree view of tests, each with a green checkmark in the right margin. The tests are grouped into several categories:

- Common Mode Regular**
 - HFR5-1-20: eARC Discovery With COMMA Width Margining
 - HFR5-1-21: Command Behavior With Bit Time Margining
 - HFR5-1-22: TX gets <NACK> indicating eARC RX Busy
 - HFR5-1-23: TX gets Common Mode Slow Response
- Common Mode Irregular**
 - HFR5-1-24: eARC TX gets Timeout during Heartbeat
 - HFR5-1-25: eARC TX gets Heartbeat Disconnect
 - HFR5-1-26: eARC TX gets HPD LOW Disconnect
 - HFR5-1-50: eARC TX Responds <RETRY> to Read Data Packet With Uncorrectable ECC Error
 - HFR5-1-55: eARC TX gets Heartbeat Failure during Discovery
- CDS/Status**
 - HFR5-1-35: eARC TX Reads Capabilities Data Structure at startup
 - HFR5-1-36: eARC TX Re-reads Capabilities Data Structure when CAP_CHNG->1
- LPCM Protocol**
 - HFR5-1-28: eARC TX 2-channel LPCM Audio Packet Structure
 - HFR5-1-29: eARC TX Multi-Channel 2-channel layout LPCM Audio Packet Structure
 - HFR5-1-56: eARC TX Multi-Channel 8-channel layout LPCM Audio Packet Structure
 - HFR5-1-58: eARC TX Multi-Channel 16-channel layout LPCM Audio Packet Structure
 - HFR5-1-59: eARC TX Multi-Channel 32-channel layout LPCM Audio Packet Structure
- HPD/HDMI_HPD**
 - HFR5-1-38: eARC TX set HPD LOW when leaving Standby Test
 - HFR5-1-39: eARC TX EDID Update and HDML_HPD Test
 - HFR5-1-51: eARC TX EDID Update and HPD on CDS Change Test
- Lip-sync**
 - HFR5-1-37: eARC TX Re-reads ERX_LATENCY when STAT_CHNG->1
- LPCM Rate/Content**

A 'CLOSE' button is located at the bottom right of the window.



HDMI eARC Tx Testing

- ◆ HDMI 2.1 eARC Testing:
 - ◆ Verify eARC Tx (TV) for common mode and differential mode operation.
 - ◆ Run eARC common and differential mode compliance tests for Tx devices. Full list of tests supported.
 - ◆ Provides detailed Test Results with Pass/Fail and details for each subtest.
 - ◆ Enables compliance self-testing and/or pre-testing of eARC devices.
 - ◆ Enables export of compliance test results to share w/ colleagues.

Compliance Test Results Viewer

eARC Source (1.0) Compliance Test Results

Results Name: AA_eARC_Tx_Complete_MB Manufacturer: qd
Date Tested: August 13, 2018 9:02 AM Model Name: 980
Overall Status: **CTS 1.0 - Fail** Port Tested: 1

Test Results

Test Name / Details	Status
▶ HFR5-1-20: eARC Discovery With COMMA Width Margining	Pass
▶ HFR5-1-21: Command Behavior With Bit Time Margining	Pass
▶ HFR5-1-22: TX gets <NACK> indicating eARC RX Busy	Pass
▶ HFR5-1-23: TX gets Common Mode Slow Response	Pass
▶ HFR5-1-24: eARC TX gets Timeout during Heartbeat	Pass
▶ HFR5-1-25: eARC TX gets Heartbeat Disconnect	Pass
▶ HFR5-1-26: eARC TX gets HPD LOW Disconnect	Pass
▶ HFR5-1-50: eARC TX Responds <RETRY> to Read Data Packet With Uncorrectable ECC Error	Pass
▶ HFR5-1-55: eARC TX gets Heartbeat Failure during Discovery	Pass
Iter 01:	Pass
01: HFR5 1 55 1: No response to <eARC Write>	Pass
▶ HFR5-1-35: eARC TX Reads Capabilities Data Structure at startup	Fail
Iter 01:	Fail
01: HFR5 1 35 1: Verify CAP_CHNG_CONF behavior	Fail
Iteration 1, verify CAP_CHNG_CONF	
Collected 3523 events	
Analyzed 3523 events	
DUT took 72.013875ms from HPD=1 to issue heartbeat (maximum: 500ms)	
DUT sent HB after 4 COMMA ONs	
DUT set CAP_CHNG_CONF=1 in 353.7651ms (200ms max)	
DUT set CAP_CHNG_CONF=0 in 202.371275ms (200ms max)	
DUT started reading Capabilities Data Structure in 424.05195ms (2s max)	
▶ HFR5-1-36: eARC TX Re-reads Capabilities Data Structure when CAP_CHNG->1	Fail
▶ HFR5-1-28: eARC TX 2-channel LPCM Audio Packet Structure	Pass
▶ HFR5-1-29: eARC TX Multi-Channel 2-channel layout LPCM Audio Packet Structure	Pass
▶ HFR5-1-56: eARC TX Multi-Channel 8-channel layout LPCM Audio Packet Structure	Pass

Open ACA Data

Instrument: S59808 [10.30.196.240] Continue Test Execution Close

HDMI eARC Common Mode Configuration Sequence

- ◆ HDMI 2.1 eARC Testing:
 - ◆ Verify eARC common mode connection sequence using Aux Channel Analyzer (ACA) utility.
 - ◆ Enables export of ACA eARC Common Mode transactions to share w/ colleagues.



Bit	Name	Value	Description
0	EARC_HPDP	N(0)	
1		0	Reserved
2		0	Reserved
3	CAP_CHNG	Y(1)	
4	STAT_CHNG	Y(1)	
5		0	Reserved
6		0	Reserved
7		0	Reserved

Packet	M/S	C	Command/Data	Duration
001	M	C	01h Read	+0 us
002	S	C	04h Ack	+24 us
003	M	D	74h	+34 us
004	S	C	04h Ack	+24 us
005	M	D	D0h	+34 us
006	S	C	04h Ack	+24 us
007	M	C	10h Cont	+34 us
008	S	D	18h	+24 us
009	M	C	20h Stop	+33 us
010	S	C	04h Ack	+24 us