

quantumdata™ M42de Display Port 2.1 Video Analyzer/Generator



Key Features

- Equipped with USB-C ports and new enhanced full-size DisplayPort (DP80) connectors for Tx and Rx functions
- Fully supports UHBR sink and source testing at 10Gb/s, 13.5Gb/s and 20Gb/s lane rates with 128b/132b line coding
- Supports DP 1.4 (HBR3) source and sink testing including broad coverage for VESA compliance testing
- View incoming video and metadata (including DSC compressed) from a source device
- Capture and decode video, protocol, control packets including Display Stream Compression (DSC) and Multi-Stream Transport (MST)
- Custom video generator can test displays at HBR and UHBR lane rates with large format and image library
- Proprietary qdPrime™ test suite provides a huge library of custom tests designed to verify functionality and interoperability for both source and sink
- Generate Display Stream Compression (DSC), select patterns and configure slices and video parameters
- View and edit EDID and DPCD registers
- Monitor AUX Channel transactions while emulating a DP 1.4 or DP 2.1 source or sink
- Exclusive: T.A.P.4 passive monitoring mode provides visibility to Main Link and AUX Channel traffic for debug of interoperability issues between real DP 2.1 devices
- Test source and sink devices with Panel Replay capability
- Python-based automation API allows running compliance and custom verification tasks in unattended mode
- Support for LTTPR in non-transparent mode for 128b/132b at UHBR rates and 8b/10b encoding for lane rates up to HBR3
- View Power Delivery (PD) protocol negotiations for USB-C DP Alt Mode in the Aux Channel Analyzer utility

The Teledyne LeCroy quantumdata M42de Video Analyzer/Generator provides an unprecedented combination of functional and compliance testing for video, audio and protocol layers for DisplayPort 2.1. The M42de supports legacy DisplayPort HBR3 lane rates of 1.62, 2.7, 5.4, 8.1Gb/s and the new DP 2.1 UHBR lane rates of 10.0, 13.5 & 20.0Gb/s. Now enhanced to support DP80 connections over both USB Type-C® and full size DisplayPort cables, the M42de is your 'one-stop' solution for DP 2.1 testing and certification.

The quantumdata M42de is a highly configurable platform for testing DP 2.1 (and 1.4) source and sink devices with quick real-time views as well as full capture of main line video including meta data and AUX transactions. Invaluable for testing silicon development boards, displays, docking stations, hubs, USB-C adapters, retimers and extenders. The video generator offers a large library of standard video timings and test patterns necessary for easy verification of next generation displays.

The Passive Probe feature based on Teledyne LeCroy's cutting-edge T.A.P.4™ technology, enables full monitoring of the DisplayPort Main Link and the AUX Channel between two DisplayPort devices at the full 20 Gb/s lane rates.

Test Platform Overview

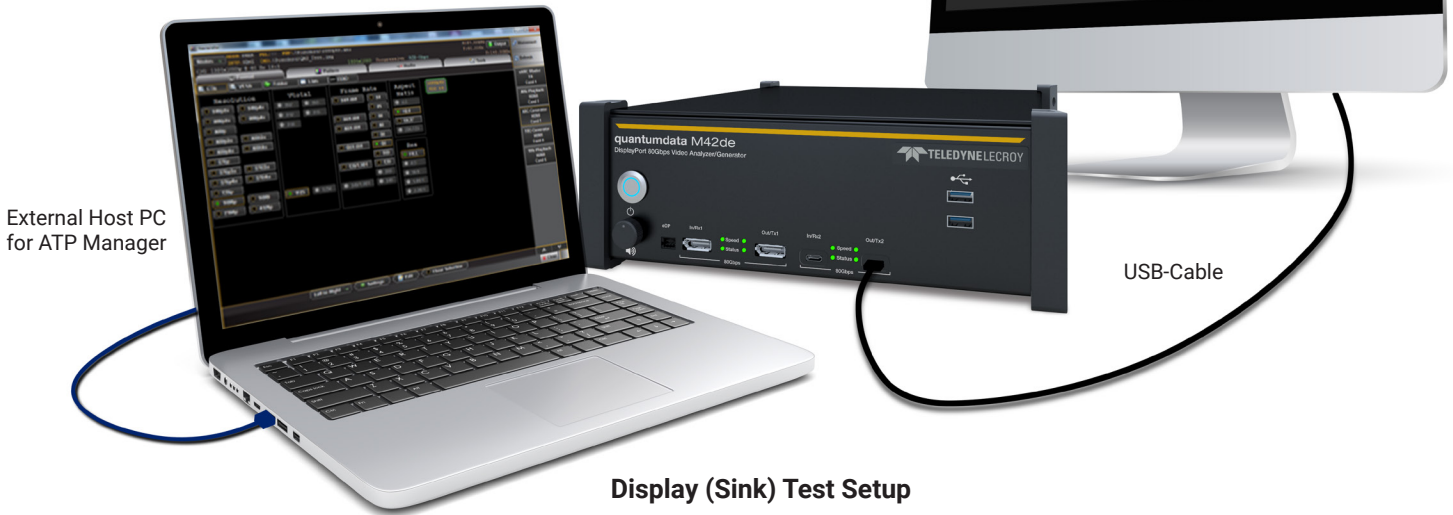
The M42de supports generation and analysis of the DisplayPort data streams through the user-friendly Video Protocol Suite Manager. The M42de features an embedded CPU (linux-based) that operates as a stand-alone platform by connecting an HDMI monitor plus keyboard/mouse (below). Optionally an external laptop can be connected directly to the unit (via RJ45 LAN port) and control the analyzer as a remote PC. Both approaches provide fast access to captured video logs up to 8GB in size.



Video Generation

The M42de supports video and audio functional testing at HBR3 / UHBR lane rates on 1, 2 or 4 lanes to support high resolution formats. Users can specify lane configurations for link training and choose from an extensive library of video formats and test patterns.

DP 2.1 Sink DUT



Display (Sink) Test Setup

Aux Channel Analyzer (ACA)

The M42de's Auxiliary Channel Analyzer (ACA) records DP AUX reads and writes to provide insights on link training, MST negotiations, HDCP, DPCD transactions, DP Alt Mode / PD negotiations and EDID exchanges. The ACA captures and timestamps these events allowing users to view each transaction fully decoded. ACA logs can be saved and distributed for off-line analysis by other team members.

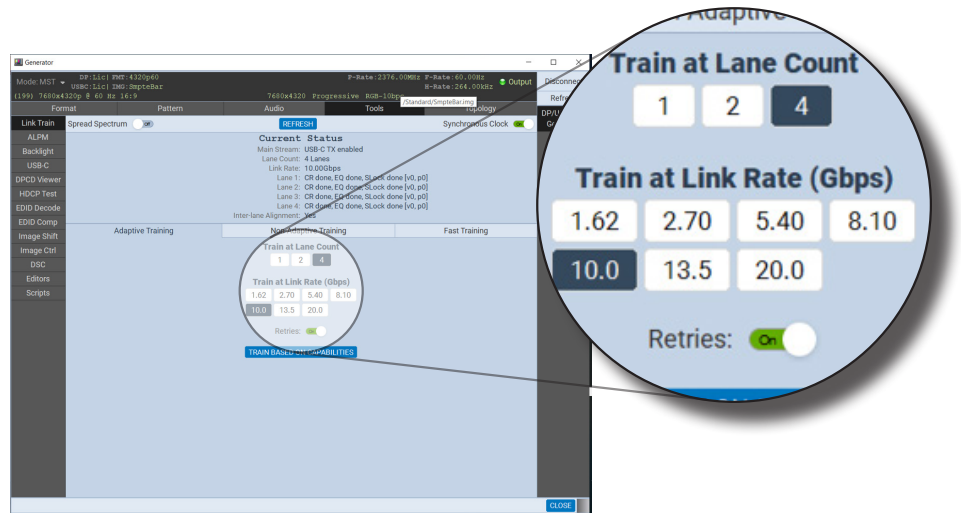
Line	Direction	Channel	Timestamp	Event	Details
86	DNAT	DPUSBC-R13	+00:13:12.664398	> R:60 DSC SUPPORT L=15	
87	DNAT	DPUSBC-R13	+00:13:12.664472	< ACK 01 21 03 7F FB 07 01 00 00 1F 0E EE 0...	
88	DNAT	DPUSBC-R13	+00:13:12.664674	> R:D eDP_CONFIGURATION_CAP L=1	
89	DNAT	DPUSBC-R13	+00:13:12.664748	< ACK 00	
90	DNAT	DPUSBC-R13	+00:13:12.664817	> R:701 EDP_GENERAL_CAPABILITY_1 L=1	
91	DNAT	DPUSBC-R13	+00:13:12.664891	< ACK 87	
92	DNAT	DPUSBC-R13	+00:13:12.664960	> R:702 EDP_BACKLIGHT_ADJ_CAPS L=1	
93	DNAT	DPUSBC-R13	+00:13:12.665034	< ACK 22	
94	DNAT	DPUSBC-R13	+00:13:12.665101	> R:725 EDP_FPMGEN_BIT_COUNT_MIN L=2	
95	DNAT	DPUSBC-R13	+00:13:12.665175	< ACK 02 0c	
96	DNAT	DPUSBC-R13	+00:13:12.665254	> R:2E RX_ALPM_CAPABILITIES L=1	
97	DNAT	DPUSBC-R13	+00:13:12.665328	< ACK 03	
98	DNAT	DPUSBC-R13	+00:13:12.665393	> W:116 RX_ALPM_CONFIGURATION L=1 01	
99	DNAT	DPUSBC-R13	+00:13:12.665475	< ACK	
100	DNAT	DPUSBC-R13	+00:13:12.665531	> R:F0000 LTTPR_FIELD_DATA_STRUCTURE_REV L=8	
101	DNAT	DPUSBC-R13	+00:13:12.665605	< ACK 20 1E 10 AA 04 10 01 05	
102	DNAT	DPUSBC-R13	+00:13:12.665801	> W:F0003 PHY_REPEATER_MODE L=1 AA	
103	DNAT	DPUSBC-R13	+00:13:12.665883	< ACK	
104	DPLT	DPUSBC-R13	+00:13:12.665999	> W:108 MAIN_LINK_CHANNEL_CODING_SET L=1 02	
105	DPLT	DPUSBC-R13	+00:13:12.666081	< ACK	
106	DPLT	DPUSBC-R13	+00:13:12.666137	> W:100 LINK_BW_SET L=1 04	
107	DPLT	DPUSBC-R13	+00:13:12.666219	< ACK	
108	DPLT	DPUSBC-R13	+00:13:12.666319	> W:101 LANE_COUNT_SET L=1 84	
109	DPLT	DPUSBC-R13	+00:13:12.666401	< ACK	
110	DPLT	DPUSBC-R13	+00:13:12.766793	> W:107 DOWNSPREAD_CTRL L=1 00	
111	DPLT	DPUSBC-R13	+00:13:12.766875	< ACK	
112	DNAT	DPUSBC-R13	+00:13:12.766978	> W:600 SINK_SET_POWER L=1 01	
113	DNAT	DPUSBC-R13	+00:13:12.767060	< ACK	
114	DNAT	DPUSBC-R13	+00:13:12.767116	> R:E TRAINING_AUX_RD_INTERVAL L=1	
115	DNAT	DPUSBC-R13	+00:13:12.767190	< ACK 81	
116	DPLT	DPUSBC-R13	+00:13:12.767303	> W:102 TRAINING_PATTERN_SET: L=1 00	
117	DPLT	DPUSBC-R13	+00:13:12.767385	< ACK	
118	DPLT	DPUSBC-R13	+00:13:12.767441	> R:205 SINK_STATUS L=1	
119	DPLT	DPUSBC-R13	+00:13:12.767515	< ACK 03	
120	DPLT	DPUSBC-R13	+00:13:12.768203	> W:108 MAIN_LINK_CHANNEL_CODING_SET L=1 02	
121	DPLT	DPUSBC-R13	+00:13:12.768285	< ACK	
122	DPLT	DPUSBC-R13	+00:13:12.768343	> W:100 LINK_BW_SET L=1 04	

Event	Bit Name	Value	Description
F0000: LTTPR_FIELD_DATA_STRUCTURE_REV	Bit Name	Value	Description
	3-0	Minor Revision Number	0
	7-4	Major Revision Number	2
F0001: Sb/10b_MAX_LINK_RATE_PHY_REPEATER	Bit Name	Value	Description
	7-0	MAX_LINK_RATE	1Eh 8.1 Gbps/lane
F0002: PHY_REPEATER_CNT	Bit Name	Value	Description
	7-0	LTTPR_Count	10h 4
F0003: PHY_REPEATER_MODE	Bit Name	Value	Description
	7-0	Mode	AAh Non-transparent
F0004: MAX_LANE_COUNT_PHY_REPEATER	Bit Name	Value	Description
	4-0	MAX_LANE_COUNT	04h Four lanes
	5	Reserved	0
	6	Reserved	0
	7	Reserved	0
F0005: PHY_REPEATER_EXTENDED_NAME_TIMEOUT	Bit Name	Value	Description
	6-0	EXT_NAME_TIMEOUT_REQUEST	16
	7	EXT_NAME_TIMEOUT_GRANTED	N(0)
F0006: MAIN_LINK_CHANNEL_CODING_PHY_REPEATER	Bit Name	Value	Description

Link Training Control and Configuration

The M42de's link training feature provides complete control of link training parameters including lane count and link rate. Convenient controls allow M42de to perform link training dynamically based on the attached device's capabilities; or forcing a specific lane count, link rate, voltage swing, and pre-emphasis.

The M42de fully supports Cable-ID for DP40 / DP80 cables. Operating as a DP sink, it can detect which cable is attached and populate the required DPCD registers. When operating as a DP Alt-mode source, the M42de will automatically read any E-Marked USB Type-C cables attached to the Tx port and configure the link appropriately.



Generate video source traffic with specific lane count, link rate and resolution with a few clicks.

Sink Tests - Control Test Pattern Panel

The M42d's Video Generator Control Test Pattern panel is the primary interface for customizing generator test functions such as Link Training, Panel Replay, Adaptive Sync, Split SDPs and Link Quality Patterns.

Split SDPs

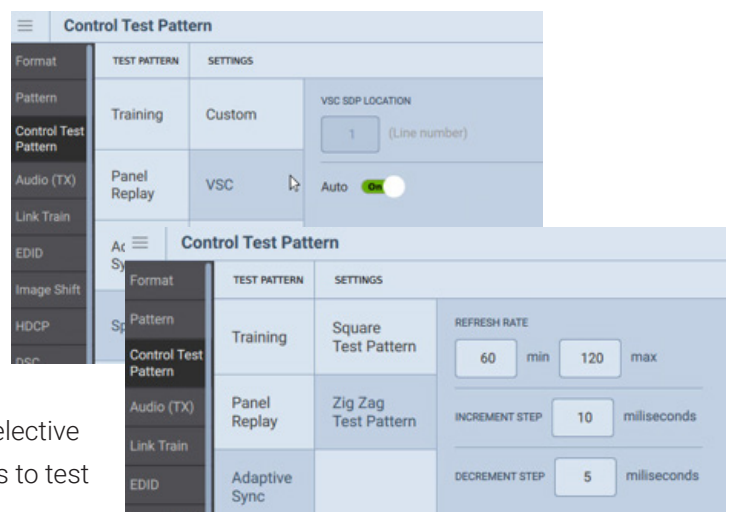
Control Test Pattern panel enables users to configure the splitting of Secondary Data Packets (SDPs). This panel includes specifying a line number for the SDP location, and optionally configuring the SDP location link clock cycles from the blanking start. The location can also be set automatically (below).

Adaptive Sync

Control Test Pattern Panel allows configuring the Adaptive Sync test patterns (ZigZag or Square Wave). Users have control of the pattern for the ramping up and down of the Adaptive Sync Refresh Rate and the time (in milliseconds) for each incremental increase or decrease in the Refresh Rate (below).

Panel Replay

For Panel Replay Tx emulation, the Control Test Pattern tab provides flexible generation including precise control of Selective Updates (SU) at specific regions/dimensions. Inject CRC errors to test recovery behaviors.

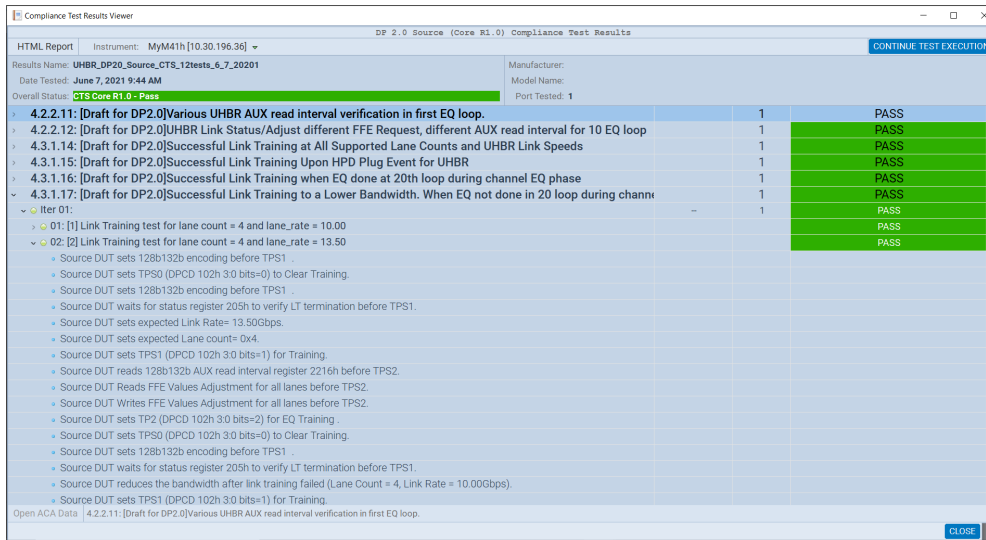


HDCP Testing

The M42de is fully approved for testing sources, sinks and branch devices for HDCP 2.2/3 compliance.

Broad Coverage of VESA Compliance Tests

The quantumdata M42de provides unmatched support for VESA compliance testing allowing developers to verify functionality, error recovery, and conformance for DisplayPort 1.4 and 2.1 sources, sinks and devices. Seamlessly integrated in the quantumdata analyzer software, the M42de connects directly to the unit-under-test (UUT) over DP40, DP80 or Type-C cables. The M42de mimics real DP source or sink behaviors while capturing the exchange and generating pass/fail reports to provide a fully turnkey test environment. A comprehensive Python-based automation API can run the entire compliance suite or custom test behaviors allowing product teams to boost their utilization and efficiency during the validation cycle.



M42de compliance option automatically logs each test step and generates pass/fail reports

The M42de is recognized by VESA as an approved test solution for both DisplayPort 1.4 and 2.1 with full coverage for Link Layer, forward error correction (FEC), display stream compression (DSC), and LTTTPR compliance. The M42de also leads the industry with tests for DP 2.1 audio, Native DisplayID and MST for both source and sink. The M42de compliance options provide comprehensive coverage allowing DisplayPort chip and device OEMs to save money by

performing self-certification in their own lab. The quantumdata team is committed to providing complete support of the DP 2.1 link and protocol Compliance Test Suite (CTS) with the regular release of software updates supporting new and updated tests.

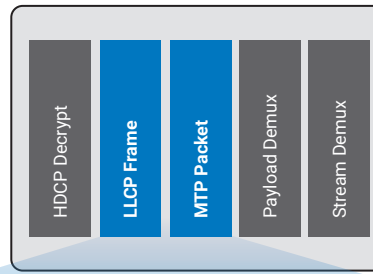
Receiver - Basic & Capture Analyzer

The M42de's Basic Analyzer allows users to view the incoming video, lanes and link rate, timing, colorimetry and various other metadata in real time at a glance. It provides instant confirmation of the negotiated resolution and a representation of the video image. The Rx port emulates any EDID to verify a source can discover and configure a wide range of displays. Similar controls are available in the DPCD Editor to allow emulation of various DP Rx parameters.

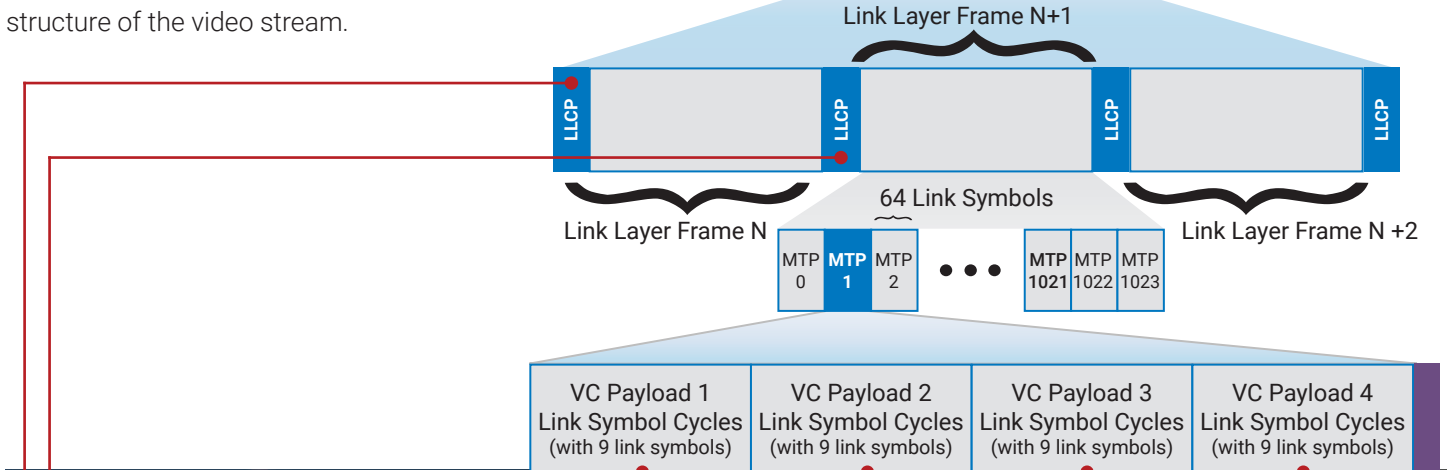


Receiver - Capture Analyzer

The deep Capture Analyzer records the high-speed link and decodes the underlying virtual channels to provide deep insight into the data, control symbols, video, metadata and protocol events (shown below). The Event Plot window provides a graphical resizable timeline offering quick insights into the sequence and structure of the video stream.



Link Layer Functional Block



The screenshot shows the DP Capture Viewer interface. The top panel displays 'Events/Data' for 'ForDemoUHBR13.5'. The main area shows a timeline with a 'Data' window and a 'VC Payloads' window. The 'VC Payloads' window shows a table of data for VC Payload 1, 2, 3, and 4, with columns for Offset, L0, L1, L2, and L3. The 'Data' window shows a series of vertical bars representing link symbols. The 'VC Payloads' window shows a detailed view of the VC Payloads, with a table of data for VC Payload 1, 2, 3, and 4, and a 'CLOSE' button at the bottom right.

Offset	L0	L1	L2	L3
+62	00000000	00000000	00000000	00000000
+63	00000000	00000000	00000000	00000000
+64	00000000	00000000	00000000	00000000
+65	00000000	00000000	00000000	00000000
+66	00000000	00000000	00000000	00000000
+67	B4101084	B4101084	B4101084	B4101084
+68	10B41010	10B41010	10B41010	10B41010
+69	1010B410	1010B410	1010B410	1010B410
+70	B4101084	B4101084	B4101084	B4101084
+71	10B41010	10B41010	10B41010	10B41010
+72	1010B410	1010B410	1010B410	1010B410
+73	B4101084	B4101084	B4101084	B4101084
+74	10B41010	10B41010	10B41010	10B41010
+75	1010B410	1010B410	1010B410	1010B410
+76	VCPF	VCPF	VCPF	VCPF
+77	1010B410	1010B410	1010B410	1010B410
+78	B4101084	B4101084	B4101084	B4101084
+79	10B41010	10B41010	10B41010	10B41010
+80	1010B410	1010B410	1010B410	1010B410
+81	B4101084	B4101084	B4101084	B4101084
+82	10B41010	10B41010	10B41010	10B41010
+83	1010B410	1010B410	1010B410	1010B410
+84	B4101084	B4101084	B4101084	B4101084
+85	1010B410	1010B410	1010B410	1010B410
+86	B4101084	B4101084	B4101084	B4101084
+87	10B41010	10B41010	10B41010	10B41010
+88	1010B410	1010B410	1010B410	1010B410
+89	B4101084	B4101084	B4101084	B4101084
+90	10B41010	10B41010	10B41010	10B41010
+91	1010B410	1010B410	1010B410	1010B410
+92	B4101084	B4101084	B4101084	B4101084
+93	10B41010	10B41010	10B41010	10B41010
+94	1010B410	1010B410	1010B410	1010B410
+95	B4101084	B4101084	B4101084	B4101084
+96	10B41010	10B41010	10B41010	10B41010
+97	1010B410	1010B410	1010B410	1010B410
+98	B4101084	B4101084	B4101084	B4101084
+99	10B41010	10B41010	10B41010	10B41010
+100	1010B410	1010B410	1010B410	1010B410
+101	B4101084	B4101084	B4101084	B4101084
+102	10B41010	10B41010	10B41010	10B41010
+103	00000000	00000000	00000000	00000000
+104	00000000	00000000	00000000	00000000
+105	00000000	00000000	00000000	00000000
+106	00000000	00000000	00000000	00000000
+107	00000000	00000000	00000000	00000000

Complete visibility into Multi-Stream Transport virtual channels including meta data, control and the logical video streams

View the underlying virtual channels with a single click

Panel Replay Rx Testing

Panel Replay Rx emulation now features an improved frame view allowing users to see the Selective Update regions captured during each frame including all VSC SDPs making it easy to see changes from the previous frame. The transaction list keeps a tally of all the VSC metadata packets. Recent improvements include "Show PR in remote frame buffer" which lets users see the overlaid SU region on the image in the Remote Frame buffer. All the critical AUX transactions for discovery and configuration of Panel Replay are also decoded.

qdPrime™ Automated Test Suite

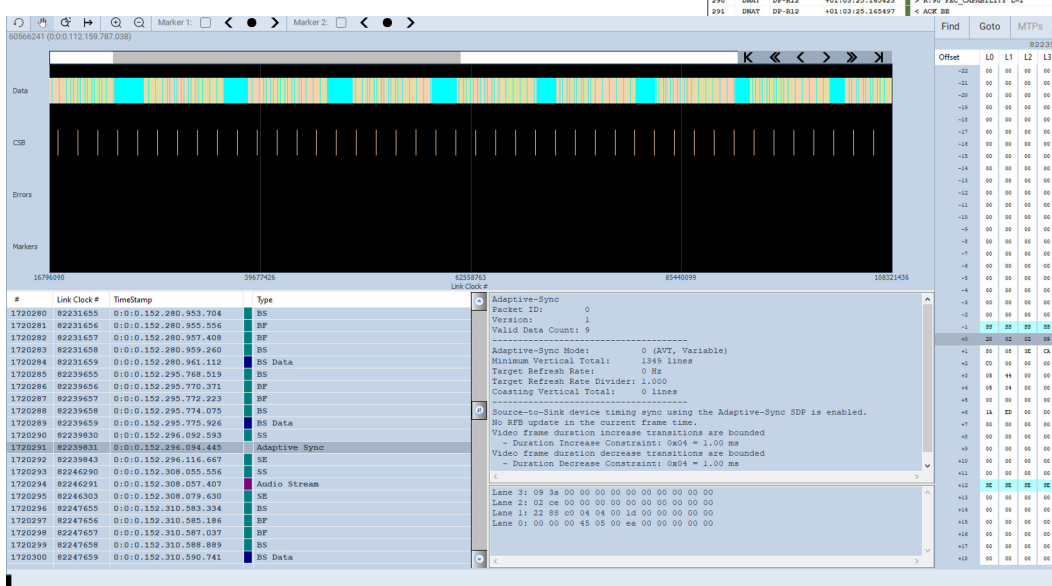
The qdPrime™ test suite provides a huge library of proprietary tests designed to verify DisplayPort functionality and interoperability for both sources and sinks. This optional feature systematically tests different combinations of lane-width, link rate, timing, refresh-rate, color-space, and bit depth to ensure devices operate properly with the DisplayPort 2.1 ecosystem. Each individual test generates a pass/fail result with detailed logs to provide a repeatable snapshot of device interoperability.

eDP Support

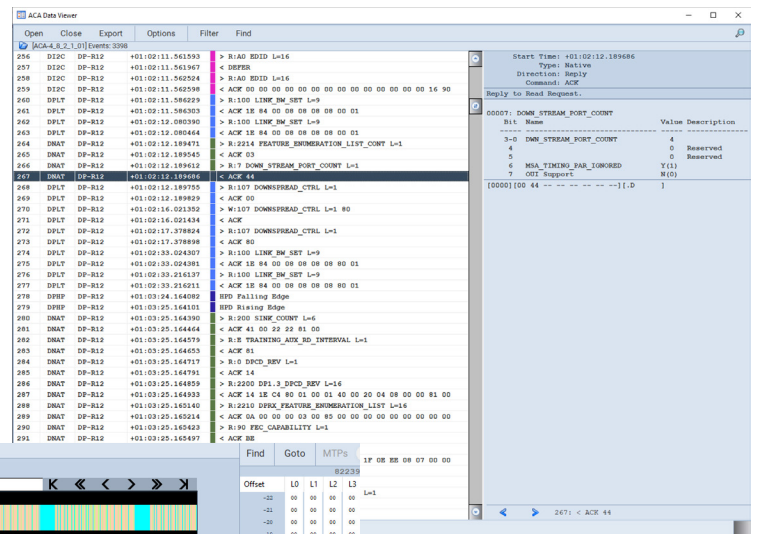
The M42de has improved support for Embedded DisplayPort (eDP) with features like ALPM, AUX-less ALPM, alternate scrambler seed, and Tx backlight control. It excels in fast link training across all VESA recommended eDP link rates, making it a top choice for testing both sources and panels. Additionally, the new 30-pin and 40-pin eDP adapters simplify the connection of eDP 1.5a source and sink devices to the M42de platforms, ensuring accuracy and convenience.

Adaptive Sync Functional Testing

The M42de now supports testing of Adaptive Sync-capable source and sink devices for HBR3 with UHBR in active development. The Adaptive Sync analyzer for source testing enables viewing variations in the vertical blanking to lower the refresh rate. The Adaptive Sync video generator for testing displays enables sending different test patterns that increase or decrease the vertical blanking to verify the refresh rate of the display.



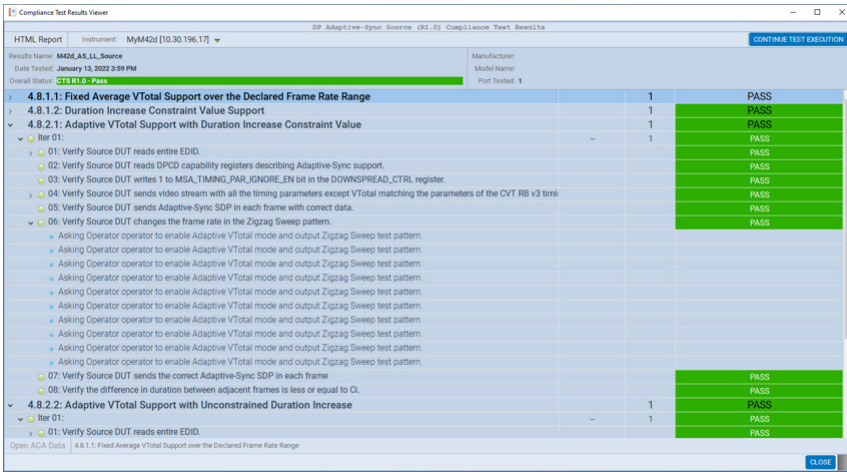
View the Adaptive Sync variations in the vertical blanking using the Capture Analyzer



View Adaptive Sync discovery and configuration transactions occurring over AUX with the Aux Channel Analyzer

Adaptive Sync Compliance Testing

The M42de supports Adaptive Sync compliance testing for both source and sink devices. Sample output provides clear summary of the test result with easy drill-down on each assertion. Fully supports HBR3 with UHBR support in active development. Adaptive Sync compliance test (left) verifies the source can operate in Adaptive VTotal mode (unconstrained) with correct CVT timing parameters.



Source Link Layer Compliance

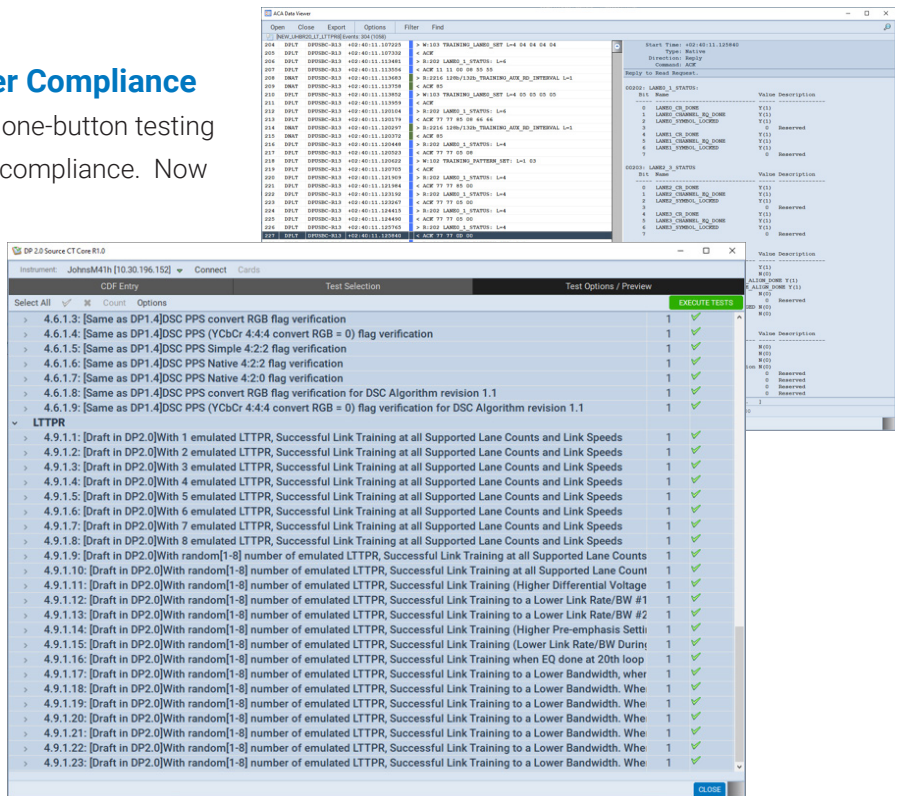
The DP source link layer compliance option is ideal for pre-testing HBR3 or UHBR-capable devices prior to submission to an Authorized Test Center. Pre-testing is considered a critical step in assuring a smooth certification process. The optional compliance test packages allow users to view detailed results and help pinpoint the cause of any failures. AUX channel traces are also saved during Link Layer testing to provide a reliable record of AUX transactions.

Sink Link Layer & EDID Compliance

The DP sink EDID/DisplayID and Link Layer compliance option fully supports DP 1.4 certification and a growing list of DP 2.1 tests. Covering dozens of test cases and hundreds of assertions, the link layer CTS package is foundational for any engineering verification test effort. With essential tests for critical functions including training, forward error correction (FEC), power management and multi-byte AUX transactions, this base package is the starting point for comprehensive test coverage.

LTPPR-Capable Source, Sink & Retimer Compliance

The quantumdata M42de provides automated, one-button testing of Link Training Tunable Phy Repeater (LTPPR) compliance. Now with specific tests for HBR3 and UHBR-capable DisplayPort source, sink and retimer devices, the M42de mimics real LTPPR network behaviors to verify that sources can properly configure and link train in both transparent and non-transparent modes. Simple pass/fail reports are automatically generated and detailed AUX logs are captured which are invaluable for understanding issues during clock data switch phase, equalization, or inter-lane alignment.



Simple pass/fail reports are automatically generated and detailed AUX logs allow quick insight into compliance issues

Specifications

DisplayPort 2.1 Capabilities	
Version	DisplayPort 2.1 (and DP 1.4)
Standard Video Formats	VESA, CTA
Protocols and Line Coding	DP, DSC, FEC, MST, SSC, SDP with 8b/10b and 128b/132b encoding (LTTTPR, Panel Replay)
Video Data Rates	1.62, 2.7, 5.4, 8.1, 10.0, 13.5 & 20 Gb/s; 1, 2, 4 Lanes
Video Encoding/Color Depths	RGB, YCbCr - 8, 10, 12, 16 bits
Video Sampling Modes	4:4:4, 4:2:2, 4:2:0
HDCP	Versions 1.3 and 2.3
Audio	8 Channel LPCM programmable sine wave
Capture Memory	8 GBytes

Connectors - Front	
DP Standard	Tx (1) Enhanced DP80 full-size; Rx (1) Enhanced DP80 full-size
USB-C	Tx (1) USB-C with DP Alt Mode; Rx (1) USB-C with DP Alt Mode
eDP Header	Pins to access eDP Tx backlight controls
USB (2)	For connecting keyboard and mouse for software interface control and external storage media

Connectors - Back	
HDMI Standard	Admin port for connecting external HDMI UHD
USB/USB-C (2 ea.)	Type-C and Type-A for mouse and keyboard
RJ45	Ethernet for connecting to network or host PC running ATP
RCA	SPDIF IN - OUT

Physical/Electric/Admin	
Power	100-240 VAC, 50-60 Hz, 200 Watts
Size / Weight	Height: 3.44 in. (8.74 cm) Width: 9.57 in. (24.30 cm) Depth: 10.94 in. (27.79 cm) - 7.6 LBS; 5.057 Kg
Rack mountable	2 RU mounts in 19-inch rack with rack mounting brackets
Internal speaker	Speaker with volume control for monitoring incoming LPCM audio
Command Line Control	Ethernet (RJ-45) for external GUI
System Control	External PC connected over LAN to Ethernet RJ45, VNC or Keyboard/mouse and 4K TV at Admin HDMI port
Environmental	Operating Temp: 32 to 104 (F); 0 to 40 (C)

Ordering Information

Product Description

M42de UHBR Video Analyzer/Generator (Hardware system with basic generation and analysis for HBR3 and UHBR rates)
M42de HBR3 Video Analyzer/Generator (Hardware system with basic generation and analysis for HBR3 rates)

Product Code

00-00263
00-00264

Options

M42de / M42d Upgrade from HBR3 systems (00-00261 or 00-00264) to enable UHBR rates	95-00221
Passive Probing Main Link and AUX Channel	95-00222
Sink Enhanced Functional test - Includes DSC, LTTTPR, Panel Replay & Adaptive Sync Functional Tests	95-00225
Source Enhanced Functional test – Includes DSC, Capture Analysis, LTTTPR, Panel Replay, Adaptive Sync Functional	95-00226
DP 1.4 Sink EDID/DisplayID compliance tests (requires 95-00225)	95-00227
DP 1.4 Source EDID/DisplayID compliance tests (requires 95-00226)	95-00228
DP 1.4/2.1 Source Link Layer & (MST in development) compliance tests (requires 95-00226)	95-00232
DP 1.4/2.1 Sink Link Layer & (MST in development) compliance tests (requires 95-00225)	95-00233
DP 1.4/2.1 DSC/FEC Source compliance tests (requires 95-00226)	95-00236
DP 1.4/2.1 DSC/FEC Sink compliance tests (requires 95-00225)	95-00237
DP 1.4/2.1 LTTTPR Source compliance tests (requires 95-00226)	95-00240
DP 1.4/2.1 LTTTPR Sink compliance tests (requires 95-00225)	95-00241
DP 1.4/2.1 LTTTPR Device compliance tests (requires 95-00225 & 95-00226)	95-00242
DP 1.4/2.1 Adaptive Sync Source compliance test (support for DP 2.1 UHBR rates is future) (requires 95-00226)	95-00234
DP 1.4/2.1 Adaptive Sync Sink compliance test (support for DP 2.1 UHBR rates is future) (requires 95-00225)	95-00235
HDCP 2.3 Source compliance tests (requires 95-00226)	95-00214
HDCP 2.3 Sink compliance tests (requires 95-00225)	95-00217
qdPrime™ Source Test Suite	95-00280
qdPrime™ Sink Test Suite	95-00281
Embedded DisplayPort (eDP) Option	95-00212
eDP-to-DP 30-pin Adapter	95-00292
eDP-to-DP 40-pin Adapter	95-00293
M41x Rack-mount Kit	95-00209



Local sales offices are located throughout the world.
Visit our website to find the most convenient location.
1-800-5-LeCroy • teledynelecroy.com



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