

# M42h for HDMI 2.2 – Product Overview

April – 2025



# Teledyne HDMI Mission Statement

*Help silicon and product developers bring their next-generation video solutions to market—faster, without interoperability problems and at reduced cost*



Our solutions quicken Time-to-Insight

## HDMI 2.2 – Spec Changes

- ◆ New link rates of 16G, 20G and 24G added to support the higher aggregate link rates up to 96G.
- ◆ Support for Higher bandwidths without compression.
  - ◆ 4K@240 and 8K@60Hz with HDR10 4:4:4 at 10/12-bit deep color.
  - ◆ 8K @120Hz YCbCr 4:2:0 sampling at 10/12-bit deep color.
  - ◆ 10K @60Hz 4:2:0 sampling at 10/12-bit deep color.
  - ◆ 12K @60Hz 4:2:0 sampling at 10/12-bit deep color.
- ◆ Latency Indication Protocol for end-to-end AV sync is approved.
- ◆ New cable plug will be required. This will be mechanically backward compatible.
- ◆ New receptacle will be required as well. Cables and plugs updated to Category 4.
- ◆ Changes to TxFFE for FRL link training.
- ◆ AC coupling on HDMI Tx ports.

# M42h – Connectors – Front

## ◆ Front Chassis Connections and Controls

- ◆ USB Type A (2) – Used for administration and management of the ATP embedded GUI with a mouse and keyboard.
- ◆ LCD display – Provide status information and network configuration information.
- ◆ HDMI 48G Tx Port – HDMI Type A Cat 3.
- ◆ HDMI 48G Rx Port – HDMI Type A Cat 3.
- ◆ HDMI 96G Tx Port – HDMI Type A Cat 4.
- ◆ HDMI 96G Rx Port – HDMI Type A Cat 4.



## ◆ HDMI Tx/Rx Port LEDs.

- ◆ **Speed:** Red=TMDS, Green=FRL
- ◆ **Status:** Red=no HP/5V, Green=HP/5V
- ◆ LCD Display - Provides status information and network configuration.
  - ◆ **Page 1** - IP Address and Release:  
M42h IP address  
e.g.: 10.211.177.50  
e.g.: 7.46.02
  - ◆ **Page 2** - Date:  
e.g.: Wednesday April 01, 2025
  - ◆ **Page 3** - Format on active Tx port:  
e.g.: 48G Tx: 3840x2160p60 RGB
  - ◆ **Page 4** - eARC status on 96G Tx port:  
e.g.: disabled
  - ◆ **Page 5** - Rx Port configuration:  
e.g.: 48G Rx: TMDS
  - ◆ **Page 6** - eARC Tx on Rx Port:  
e.g.: enabled  
L-PCM 48kHz, 24-bit, 2ch, 6.144MHz clock

# M42h – HDMI Tx & Rx Connectors – Front

- ◆ HDMI 48G Tx Port – HDMI Type A Cat 3. Supports TMDS and “legacy” FRL speeds. This port is hardware-capable of FFE features in the spec. Can be AC-coupled or DC-coupled.
- ◆ HDMI 48G Rx Port – HDMI Type A Cat 3. Supports TMDS and “legacy” FRL speeds. This port is hardware-capable of adaptive EQ.

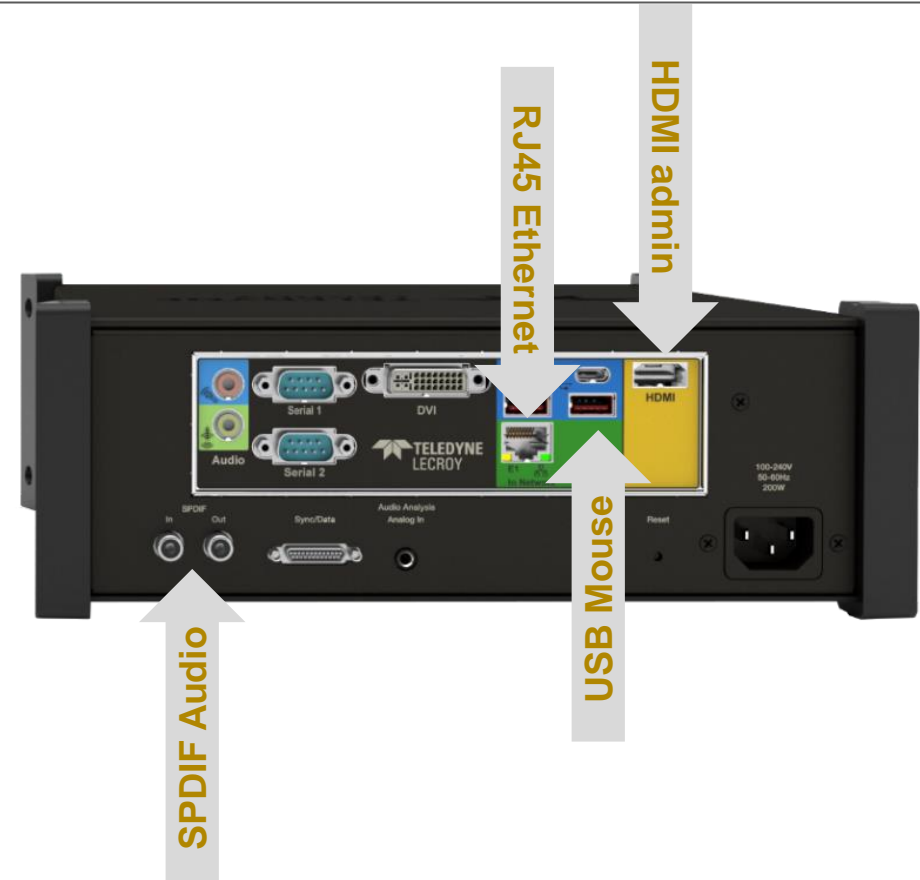


- ◆ HDMI 96G Tx Port – HDMI Type A Cat 4. Supports TMDS, “legacy” FRL (up to 48G) and the new FRL speeds up to 96G. This port is not hardware capable of supporting FFE. HDMI Cat 4 connector type. Permanently AC-coupled. This port can support passive monitoring of the DDC and CEC lines.
- ◆ HDMI 96G Rx Port – HDMI Type A Cat 4. Supports TMDS, “legacy” FRL (up to 48G) and the new FRL speeds up to 96G. This port is not hardware capable of supporting adaptive EQ. HDMI Cat 4 connector type. This port can support passive monitoring of the DDC and CEC lines.

# M42h – Connectors - Back

## ◆ Back Chassis Connections

- ◆ HDMI Admin Port – Used for administration to show the embedded ATP GUI controlled with a mouse.
- ◆ USB Type A – Use for connecting a mouse and keyboard for managing through the embedded ATP GUI.
- ◆ RJ45 connector for Ethernet/IP session for managing through the external ATP GUI.
- ◆ SPDIF In/Out for injecting and extracting SPDIF audio.
- ◆ TRS 3.5mm Stereo Audio Jack – For Audio Analysis Analog in for measuring audio latencies using microphone input.



# M42h – Comprehensive, Multi-Dimensional HDMI Test Solutions

Type of testing  
Functional, Interop, COMPLIANCE



Protocols tested

TMD5, EDID, Video, HDR, Audio, FRL, Link Train, FEC, DSC, GameVRR, eARC, HDCP, CEC

Device types tested  
Source, Sink, Repeater

- Functional Testing** – Emulation, status presentation, configurable
- Interoperability Testing** – Irregular tests, deep analysis
- Compliance Testing** – Testing to a compliance test spec for logo certification
- Fourth Dimension: Supports HDMI 1.4, HDMI 2.1, HDMI 2.2 spec tenures.**

# M42h – Roadmap and Rollout

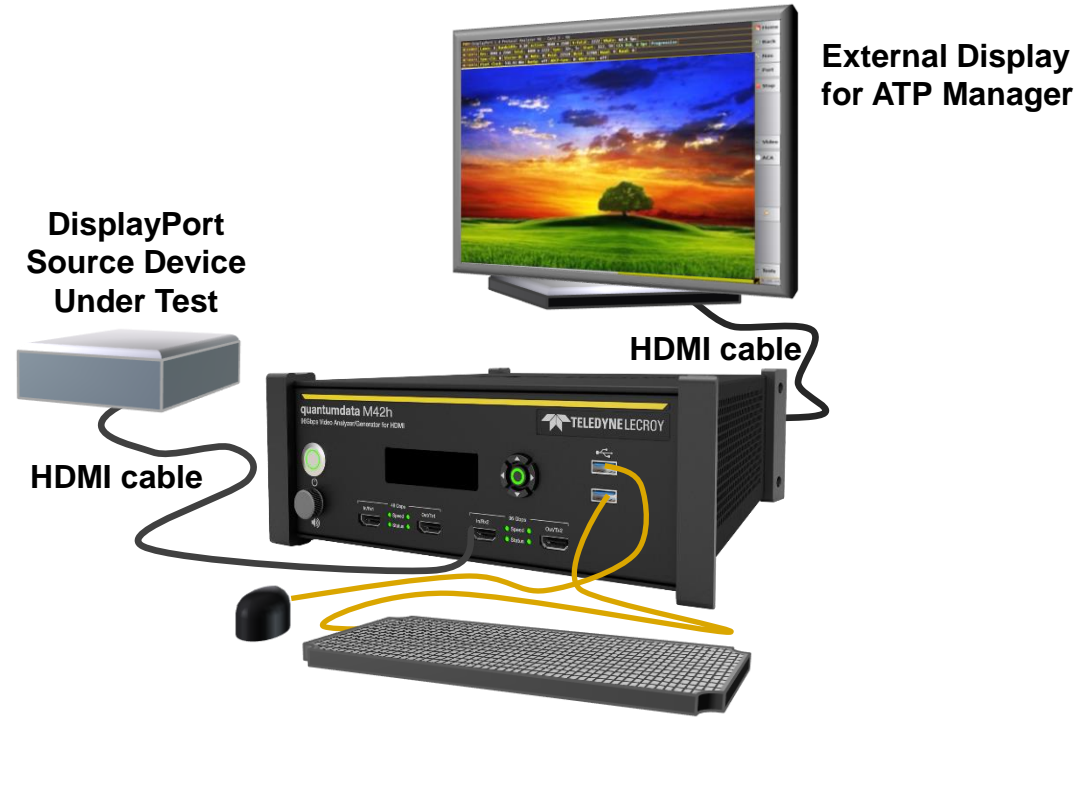
- ◆ Phase I – Release 7.48 - May 2025
  - ◆ Video Generation (Sink Testing)
    - ◆ Link training at all new FRL2 rates.
    - ◆ Transmission of existing video formats and test patterns.
    - ◆ ACA monitoring as an emulated source.
    - ◆ Reading EDID/Parsing.
    - ◆ Transmission of LPCM audio.
  - ◆ Video/Protocol Analysis (Source Testing)
    - ◆ Link training at all new higher FRL lane rates.
    - ◆ Capture analysis for new higher FRL rates.
    - ◆ ACA monitoring as an emulated sink.
    - ◆ Emulating an EDID and SCDC of a sink with the new higher FRL rates.



# M42h Administration – Embedded ATP Manager GUI (Source Test)

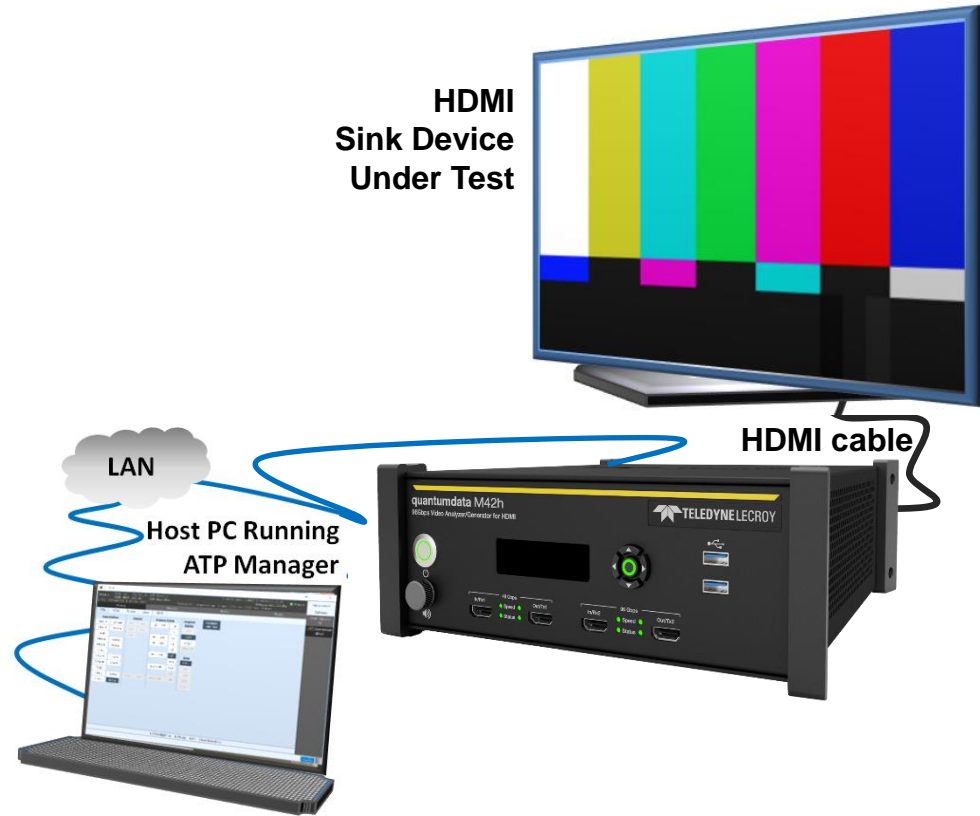
## ◆ Administration

- ◆ Use Keyboard and mouse to control ATP Manager GUI running on the connected display.



# M42h Administration – External ATP Manager GUI (Source Test)

- ◆ Administration
  - ◆ Use Windows PC as a host for the external ATP Manager GUI.



# HDMI 2.2 – M42h - Video Generator Link Training

MODE:FRL FRL:4/24G FMT:4320p60 PixClk:2376.00MHz VRate:60.00Hz HRate:264.00kHz Output

INTF:HDMI DSC:No IMG:Master eARC:On

(199) 7680x4320p @ 60 Hz 16:9 7680x4320 Progressive RGB-8bpc

Format Tools

Link Train **Current Status**

EDID Decode State :LTS\_P

EDID Comp Lanes :4

SCDC Editor Rate :24 Gbps

AFC FFE :0

Editors FRL PLL LOCKED:YES

Scripts

Auto-Train on Hot-Plug

On Off

EDID Max FRL Rate Override

Use EDID Value

Force Link Train at

FRL Off

3 Gbps @ 3 Lanes 6 Gbps @ 3 Lanes

6 Gbps @ 4 Lanes 8 Gbps @ 4 Lanes

10 Gbps @ 4 Lanes 12 Gbps @ 4 Lanes

16 Gbps @ 4 Lanes 20 Gbps @ 4 Lanes

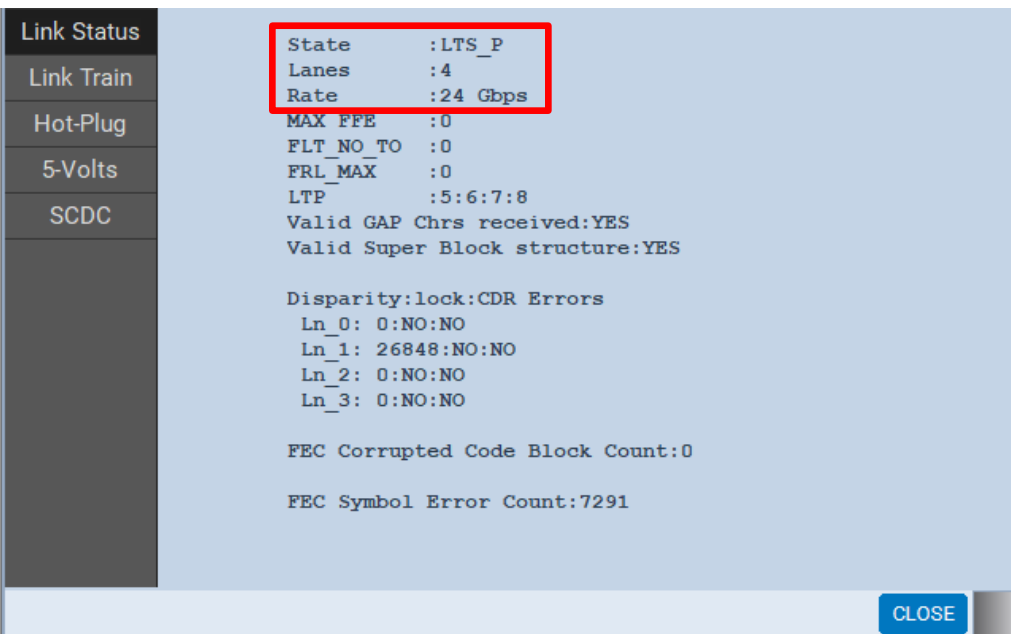
24 Gbps @ 4 Lanes

CLOSE

- ◆ Video Generator Link Training configuration screen showing 24G and other new FRL2 rates.

# HDMI 2.2 – M42h – Analyzer Sink Status Screen

- ◆ Analyzer Link Status screen showing 24G link training status.



The screenshot displays the Analyzer Sink Status screen with a sidebar on the left containing menu items: Link Status, Link Train, Hot-Plug, 5-Volts, and SCDC. The main area shows the following text:

```
State      :LTS_P
Lanes     :4
Rate      :24 Gbps
MAX_FFE   :0
FLT_NO_TO :0
FRL_MAX   :0
LTP       :5:6:7:8
Valid GAP Chrs received:YES
Valid Super Block structure:YES

Disparity:lock:CDR Errors
Ln_0: 0:NO:NO
Ln_1: 26848:NO:NO
Ln_2: 0:NO:NO
Ln_3: 0:NO:NO

FEC Corrupted Code Block Count:0

FEC Symbol Error Count:7291
```

A red box highlights the first three lines of the status information. A "CLOSE" button is located at the bottom right of the screen.

# HDMI 2.2 – M42h – Video Generator Format Selection Screen

MODE:FRL FRL:4/24G FMT:4320p60 PixClk:2376.00MHz VRate:60.00Hz HRate:264.00kHz Output

INTF:HDMI DSC:No IMG:ColorBar eARC:On

(199) 7680x4320p @ 60 Hz 16:9 7680x4320 Progressive RGB-8bpc

Format Tools

CTA	VESA	OVT	Folder	Lists	EDID&NDID	
<b>Resolution</b>		<b>Vtotal</b>		<b>Frame Rate</b>		<b>Aspect Ratio</b>
240p2x	240p4x	262	263	24/1.001	24	4:3
288p2x	288p4x	312	313		25	
480p		314		30/1.001	30	16:9
480p2x	480i2x			48/1.001	48	64:27
480p4x	480i4x				50	256:135
576p				60/1.001	60	<b>Box</b>
576p2x	576i2x				100	<b>FILL</b>
576p4x	576i4x			120/1.001	120	4:3
720p					144	16:9
1080p	1080i	1125	1250		200	1.85:1
2160p	4320p	2000	2040	240/1.001	240	2.39:1

4320p60 VIC 199

Left to Right Settings Edit Clear Selection

CLOSE

- ◆ Video Generator Format Selection screen showing 8K format being selected.
- ◆ 10K and 12K formats will also be available.

# HDMI 2.2 – M42h - EDID

The screenshot displays the EDID decode interface for a connected sink. The top status bar shows: MODE:FRL FRL:4/24G FMT:1080p60 PixClk:148.50MHz VRate:60.00Hz HRate:67.50kHz Output. Below this, the mode is identified as (16) 1920x1080p @ 60 Hz 16:9, 1920x1080 Progressive RGB-8bpc. The interface includes sections for Link Train, EDID Decode (Block #01), EDID Comp, SCDC Editor, AFC, Editors, and Scripts. The AFC section is highlighted with a red box and contains the following data:

- Version: 1
- Max\_TMDS\_Character\_Rate: 1200 MHz
- Max\_FRL\_Rate: 24 Gbps @ 4 Lanes

The Scripts section lists various capabilities: Y: SCDC\_Present, N: RR\_Capable, N: CABLE\_STATUS, N: CCBPCI, Y: LTE\_340MHz\_scramble, N: Independent\_view, N: Dual\_View, N: 3D\_OSD\_Disparity, N: UHD\_VIC, Y: DC\_48bit\_420, Y: DC\_36bit\_420, and Y: DC\_30bit\_420. The bottom navigation bar shows Block 2/2 and Page 5/13. A 'CLOSE' button is located at the bottom right of the interface.

- ◆ EDID Decode Screen showing 24G capability on the connected sink.

# HDMI 2.2 – M42h – Aux Channel Analyzer Capture

The screenshot shows the ACA Data Viewer interface. The main window displays a list of events for an LT\_96G\_Combined\_Example. The detailed view on the right shows the SCDC structure, including the Status Flags 0 field. A red box highlights the following bits:

Bit	Name	Value	Description
5	Reserved	0	Reserved
6	FRL_ready	Y(1)	
7	DSC_DecodeFail	N(0)	

- ◆ Screen example showing FRL Link Training transactions captured at 24G per lane, 96G aggregate.
- ◆ Showing FRL Ready flag set.

# HDMI 2.2 – M42h – Aux Channel Analyzer Capture

ACA Data Viewer

Open Close Export Options Filter Find

LT\_96G\_Combined\_Example Events: 68 (4267)

Time	Channel	Direction	Rate	Description
9	EDDC	HDMI-R10	+02:42:19.459449	W Segment 00 (97.14 kbps)
10	EDDC	HDMI-R10	+02:42:19.459777	R EDID 80 (97.14 kbps)
11	EDDC	HDMI-R10	+02:42:19.459941	< 128 bytes (97.14 kbps)
12	SCDC	HDMI-R10	+02:42:19.521708	R Sink Version (97.14 kbps)
13	SCDC	HDMI-R10	+02:42:19.522035	< 01 (97.14 kbps)
14	SCDC	HDMI-R10	+02:42:19.522199	W Source Version 01 (97.14 kbps)
15	SCDC	HDMI-R10	+02:42:19.522527	R Source Test Configuration (97.14 kbps)
16	SCDC	HDMI-R10	+02:42:19.522691	< 00 (97.14 kbps)
17	SCDC	HDMI-R10	+02:42:19.523018	R Status_Flags_0 (97.14 kbps)
18	SCDC	HDMI-R10	+02:42:19.523182	< 41 (97.14 kbps)
19	SCDC	HDMI-R10	+02:42:19.523346	W Config_1 09 (97.14 kbps)
20	SCDC	HDMI-R10	+02:42:19.523674	W Config_0 00 (97.14 kbps)
21	SCDC	HDMI-R10	+02:42:19.524001	R Update_0 (97.14 kbps)
22	SCDC	HDMI-R10	+02:42:19.524165	< 01 (97.14 kbps)
23	SCDCV	HDMI-R10	+02:42:19.526459	Update Reads 9: 01
24	SCDC	HDMI-R10	+02:42:19.549068	R Update_0 (97.14 kbps)
25	SCDC	HDMI-R10	+02:42:19.549232	< 21 (97.14 kbps)
26	SCDC	HDMI-R10	+02:42:19.549560	R Status_Flags_1 (97.14 kbps)
27	SCDC	HDMI-R10	+02:42:19.549724	< 65 (97.14 kbps)
28	SCDC	HDMI-R10	+02:42:19.549888	R Status_Flags_2 (97.14 kbps)
29	SCDC	HDMI-R10	+02:42:19.550215	< 87 (97.14 kbps)
30	SCDC	HDMI-R10	+02:42:19.550379	R Update_0 (97.14 kbps)
31	SCDC	HDMI-R10	+02:42:19.550543	< 21 (97.14 kbps)
32	SCDC	HDMI-R10	+02:42:19.550707	W Update_0 21 (97.14 kbps)
33	SCDC	HDMI-R10	+02:42:19.553164	R Update_0 (97.14 kbps)
34	SCDC	HDMI-R10	+02:42:19.553328	< 00 (97.14 kbps)
35	SCDCV	HDMI-R10	+02:42:19.555622	Update Reads 10: 00
36	SCDC	HDMI-R10	+02:42:19.580689	R Update_0 (97.14 kbps)
37	SCDC	HDMI-R10	+02:42:19.580853	< 23 (97.14 kbps)
38	SCDC	HDMI-R10	+02:42:19.581181	R Status_Flags_1 (97.14 kbps)
39	SCDC	HDMI-R10	+02:42:19.581344	< 00 (97.14 kbps)
40	SCDC	HDMI-R10	+02:42:19.581508	R Status_Flags_2 (97.14 kbps)
41	SCDC	HDMI-R10	+02:42:19.581672	< 00 (97.14 kbps)
42	SCDC	HDMI-R10	+02:42:19.582000	R Update_0 (97.14 kbps)
43	SCDC	HDMI-R10	+02:42:19.582164	< 23 (97.14 kbps)
44	SCDC	HDMI-R10	+02:42:19.582328	W Update_0 23 (97.14 kbps)
45	SCDC	HDMI-R10	+02:42:19.582655	R Update_0 (97.14 kbps)
46	SCDC	HDMI-R10	+02:42:19.582819	< 03 (97.14 kbps)
47	SCDCV	HDMI-R10	+02:42:19.585113	Update Reads 10: 03
48	SCDC	HDMI-R10	+02:42:19.610180	R Update_0 (97.14 kbps)
49	SCDC	HDMI-R10	+02:42:19.610344	< 13 (97.14 kbps)
50	SCDC	HDMI-R10	+02:42:19.610671	W Update_0 13 (97.14 kbps)

Type: SCDC  
Start Time: +02:42:19.523346  
Duration: 328 to 492 us  
Maximum I2C Rate: 97.14 kbps  
Write, 1 byte  
31h: Config\_1

Bit	Name	Value	Description
3-0	FRL_Rate	9	FRL, 24 Gps/lane, 4 Lanes
7-4	FFE_Levels	0	

\* START \*  
0000 A8 31 09 | . . .  
\* STOP \*

19: W Config\_1 09 (97.14 kbps)

- ◆ Screen example showing FRL Link Training transactions capture at 24G per lane, 96G aggregate.
- ◆ Showing FRL rate being configured.

# HDMI 2.2 – M42h – Aux Channel Analyzer Capture

ACA Data Viewer

Open Close Export Options Filter Find

[LT\_96G\_Combined\_Example] Events: 68 (4267)

Time	Channel	Data
0	SCDC HDMI-R10	+02:41:11.783912 R Update_0 (97.14 kbps)
1	SCDC HDMI-R10	+02:41:11.784076 < 43 (97.14 kbps)
2	SCDCU HDMI-R10	+02:41:11.786370 Update Reads 24: 43
3	SCDC HDMI-R10	+02:41:11.846826 R Update_0 (97.14 kbps)
4	SCDC HDMI-R10	+02:42:19.297742 R Update_0 (97.14 kbps)
5	SCDC HDMI-R10	+02:42:19.297906 < 01 (97.14 kbps)
6	EDDC HDMI-R10	+02:42:19.347876 W Segment 00 (97.14 kbps)
7	EDDC HDMI-R10	+02:42:19.348040 R EDID 00 (97.14 kbps)
8	EDDC HDMI-R10	+02:42:19.348204 < 128 bytes (97.14 kbps)
9	EDDC HDMI-R10	+02:42:19.459449 W Segment 00 (97.14 kbps)
10	EDDC HDMI-R10	+02:42:19.459777 R EDID 80 (97.14 kbps)
11	EDDC HDMI-R10	+02:42:19.459941 < 128 bytes (97.14 kbps)
12	SCDC HDMI-R10	+02:42:19.521708 R Sink Version (97.14 kbps)
13	SCDC HDMI-R10	+02:42:19.522035 < 01 (97.14 kbps)
14	SCDC HDMI-R10	+02:42:19.522199 W Source Version 01 (97.14 kbps)
15	SCDC HDMI-R10	+02:42:19.522527 R Source Test Configuration (97.14 kbps)
16	SCDC HDMI-R10	+02:42:19.522691 < 00 (97.14 kbps)
17	SCDC HDMI-R10	+02:42:19.523018 R Status_Flags_0 (97.14 kbps)
18	SCDC HDMI-R10	+02:42:19.523182 < 41 (97.14 kbps)
19	SCDC HDMI-R10	+02:42:19.523346 W Config_1 09 (97.14 kbps)
20	SCDC HDMI-R10	+02:42:19.523674 W Config_0 00 (97.14 kbps)
21	SCDC HDMI-R10	+02:42:19.524001 R Update_0 (97.14 kbps)
22	SCDC HDMI-R10	+02:42:19.524165 < 01 (97.14 kbps)
23	SCDCU HDMI-R10	+02:42:19.526459 Update Reads 9: 01
24	SCDC HDMI-R10	+02:42:19.549068 R Update_0 (97.14 kbps)
25	SCDC HDMI-R10	+02:42:19.549232 < 21 (97.14 kbps)
26	SCDC HDMI-R10	+02:42:19.549560 R Status_Flags_1 (97.14 kbps)
27	SCDC HDMI-R10	+02:42:19.549724 < 65 (97.14 kbps)
28	SCDC HDMI-R10	+02:42:19.549888 R Status_Flags_2 (97.14 kbps)
29	SCDC HDMI-R10	+02:42:19.550215 < 87 (97.14 kbps)
30	SCDC HDMI-R10	+02:42:19.550379 R Update_0 (97.14 kbps)
31	SCDC HDMI-R10	+02:42:19.550543 < 21 (97.14 kbps)
32	SCDC HDMI-R10	+02:42:19.550707 W Update_0 21 (97.14 kbps)
33	SCDC HDMI-R10	+02:42:19.553164 R Update_0 (97.14 kbps)
34	SCDC HDMI-R10	+02:42:19.553328 < 00 (97.14 kbps)
35	SCDCU HDMI-R10	+02:42:19.555622 Update Reads 10: 00
36	SCDC HDMI-R10	+02:42:19.580689 R Update_0 (97.14 kbps)
37	SCDC HDMI-R10	+02:42:19.580853 < 23 (97.14 kbps)
38	SCDC HDMI-R10	+02:42:19.581181 R Status_Flags_1 (97.14 kbps)
39	SCDC HDMI-R10	+02:42:19.581344 < 00 (97.14 kbps)
40	SCDC HDMI-R10	+02:42:19.581508 R Status_Flags_2 (97.14 kbps)
41	SCDC HDMI-R10	+02:42:19.581672 < 00 (97.14 kbps)

Type: SCDC  
Start Time: +02:42:19.550215  
Duration: 164 to 328 us  
Maximum I2C Rate: 97.14 kbps

Read, 1 byte  
42h: Status\_Flags\_2

Bit Name	Value	Description
3-0 Ln2_LTP_req	7	LFSR 2
7-4 Ln3_LTP_req	8	LFSR 3

\* START \*  
0000 A9 87-  
\* STOP \*

29: < 87 (97.14 kbps)

- ◆ Screen example showing FRL Link Training transactions capture at 24G per lane, 96G aggregate.
- ◆ Showing Link Training pattern being configured.

# HDMI 2.2 – M42h – Aux Channel Analyzer Capture

ACA Data Viewer

Open Close Export Options Filter Find

[LT\_96G\_Combined\_Example] Events: 68 (4267)

Time	Channel	Data
6	EDDC HDMI-R10	+02:42:19.347876 W Segment 00 (97.14 kbps)
7	EDDC HDMI-R10	+02:42:19.348040 R EDID 00 (97.14 kbps)
8	EDDC HDMI-R10	+02:42:19.348204 < 128 bytes (97.14 kbps)
9	EDDC HDMI-R10	+02:42:19.459449 W Segment 00 (97.14 kbps)
10	EDDC HDMI-R10	+02:42:19.459777 R EDID 80 (97.14 kbps)
11	EDDC HDMI-R10	+02:42:19.459941 < 128 bytes (97.14 kbps)
12	SCDC HDMI-R10	+02:42:19.521708 R Sink Version (97.14 kbps)
13	SCDC HDMI-R10	+02:42:19.522035 < 01 (97.14 kbps)
14	SCDC HDMI-R10	+02:42:19.522199 W Source Version 01 (97.14 kbps)
15	SCDC HDMI-R10	+02:42:19.522527 R Source Test Configuration (97.14 kbps)
16	SCDC HDMI-R10	+02:42:19.522691 < 00 (97.14 kbps)
17	SCDC HDMI-R10	+02:42:19.523018 R Status_Flags_0 (97.14 kbps)
18	SCDC HDMI-R10	+02:42:19.523182 < 41 (97.14 kbps)
19	SCDC HDMI-R10	+02:42:19.523346 W Config_1 09 (97.14 kbps)
20	SCDC HDMI-R10	+02:42:19.523674 W Config_0 00 (97.14 kbps)
21	SCDC HDMI-R10	+02:42:19.524001 R Update_0 (97.14 kbps)
22	SCDC HDMI-R10	+02:42:19.524165 < 01 (97.14 kbps)
23	SCDCU HDMI-R10	+02:42:19.526459 Update Reads 9: 01
24	SCDC HDMI-R10	+02:42:19.549068 R Update_0 (97.14 kbps)
25	SCDC HDMI-R10	+02:42:19.549232 < 21 (97.14 kbps)
26	SCDC HDMI-R10	+02:42:19.549560 R Status_Flags_1 (97.14 kbps)
27	SCDC HDMI-R10	+02:42:19.549724 < 65 (97.14 kbps)
28	SCDC HDMI-R10	+02:42:19.549888 R Status_Flags_2 (97.14 kbps)
29	SCDC HDMI-R10	+02:42:19.550215 < 87 (97.14 kbps)
30	SCDC HDMI-R10	+02:42:19.550379 R Update_0 (97.14 kbps)
31	SCDC HDMI-R10	+02:42:19.550543 < 21 (97.14 kbps)
32	SCDC HDMI-R10	+02:42:19.550707 W Update_0 21 (97.14 kbps)
33	SCDC HDMI-R10	+02:42:19.553164 R Update_0 (97.14 kbps)
34	SCDC HDMI-R10	+02:42:19.553328 < 00 (97.14 kbps)
35	SCDCU HDMI-R10	+02:42:19.555622 Update Reads 10: 00
36	SCDC HDMI-R10	+02:42:19.580689 R Update_0 (97.14 kbps)
37	SCDC HDMI-R10	+02:42:19.580853 < 23 (97.14 kbps)
38	SCDC HDMI-R10	+02:42:19.581181 R Status_Flags_1 (97.14 kbps)
39	SCDC HDMI-R10	+02:42:19.581344 < 00 (97.14 kbps)
40	SCDC HDMI-R10	+02:42:19.581508 R Status_Flags_2 (97.14 kbps)
41	SCDC HDMI-R10	+02:42:19.581672 < 00 (97.14 kbps)
42	SCDC HDMI-R10	+02:42:19.582000 R Update_0 (97.14 kbps)
43	SCDC HDMI-R10	+02:42:19.582164 < 23 (97.14 kbps)
44	SCDC HDMI-R10	+02:42:19.582328 W Update_0 23 (97.14 kbps)
45	SCDC HDMI-R10	+02:42:19.582655 R Update_0 (97.14 kbps)
46	SCDC HDMI-R10	+02:42:19.582819 < 03 (97.14 kbps)
47	SCDCU HDMI-R10	+02:42:19.585113 Update Reads 10: 03

Type: SCDC  
Start Time: +02:42:19.581344  
Duration: 164 to 328 us  
Maximum I2C Rate: 97.14 kbps  
Read, 1 byte  
41h: Status\_Flags\_1

Bit Name	Value	Description
3-0 Ln0_LTP_req	0	No Pattern Requested
7-4 Ln1_LTP_req	0	No Pattern Requested

\* START \*  
0000 A9 00-  
\* STOP \*

39: < 00 (97.14 kbps)

- ◆ Screen example showing FRL Link Training transactions capture at 24G per lane, 96G aggregate.
- ◆ Indicating “No Pattern Requested” meaning link training has been completed.

# HDMI 2.2 – M42h – Aux Channel Analyzer Capture

ACA Data Viewer

Open Close Export Options Filter Find

[LT\_96G\_Combined\_Example] Events: 68 (4267)

Line	Type	Channel	Time	Value	Description
9	EDDC	HDMI-R10	+02:42:19.459449	W Segment 00	(97.14 kbps)
10	EDDC	HDMI-R10	+02:42:19.459777	R EDID 80	(97.14 kbps)
11	EDDC	HDMI-R10	+02:42:19.459941	< 128 bytes	(97.14 kbps)
12	SCDC	HDMI-R10	+02:42:19.521708	R Sink Version	(97.14 kbps)
13	SCDC	HDMI-R10	+02:42:19.522035	< 01	(97.14 kbps)
14	SCDC	HDMI-R10	+02:42:19.522199	W Source Version 01	(97.14 kbps)
15	SCDC	HDMI-R10	+02:42:19.522527	R Source Test Configuration	(97.14 kbps)
16	SCDC	HDMI-R10	+02:42:19.522691	< 00	(97.14 kbps)
17	SCDC	HDMI-R10	+02:42:19.523018	R Status_Flags_0	(97.14 kbps)
18	SCDC	HDMI-R10	+02:42:19.523182	< 41	(97.14 kbps)
19	SCDC	HDMI-R10	+02:42:19.523346	W Config_1 09	(97.14 kbps)
20	SCDC	HDMI-R10	+02:42:19.523674	W Config_0 00	(97.14 kbps)
21	SCDC	HDMI-R10	+02:42:19.524001	R Update_0	(97.14 kbps)
22	SCDC	HDMI-R10	+02:42:19.524165	< 01	(97.14 kbps)
23	SCDCU	HDMI-R10	+02:42:19.526459	Update Reads 9:	01
24	SCDC	HDMI-R10	+02:42:19.549068	R Update_0	(97.14 kbps)
25	SCDC	HDMI-R10	+02:42:19.549232	< 21	(97.14 kbps)
26	SCDC	HDMI-R10	+02:42:19.549560	R Status_Flags_1	(97.14 kbps)
27	SCDC	HDMI-R10	+02:42:19.549724	< 65	(97.14 kbps)
28	SCDC	HDMI-R10	+02:42:19.549888	R Status_Flags_2	(97.14 kbps)
29	SCDC	HDMI-R10	+02:42:19.550215	< 87	(97.14 kbps)
30	SCDC	HDMI-R10	+02:42:19.550379	R Update_0	(97.14 kbps)
31	SCDC	HDMI-R10	+02:42:19.550543	< 21	(97.14 kbps)
32	SCDC	HDMI-R10	+02:42:19.550707	W Update_0 21	(97.14 kbps)
33	SCDC	HDMI-R10	+02:42:19.553164	R Update_0	(97.14 kbps)
34	SCDC	HDMI-R10	+02:42:19.553328	< 00	(97.14 kbps)
35	SCDCU	HDMI-R10	+02:42:19.555622	Update Reads 10:	00
36	SCDC	HDMI-R10	+02:42:19.580689	R Update_0	(97.14 kbps)
37	SCDC	HDMI-R10	+02:42:19.580853	< 23	(97.14 kbps)
38	SCDC	HDMI-R10	+02:42:19.581181	R Status_Flags_1	(97.14 kbps)
39	SCDC	HDMI-R10	+02:42:19.581344	< 00	(97.14 kbps)
40	SCDC	HDMI-R10	+02:42:19.581508	R Status_Flags_2	(97.14 kbps)
41	SCDC	HDMI-R10	+02:42:19.581672	< 00	(97.14 kbps)
42	SCDC	HDMI-R10	+02:42:19.582000	R Update_0	(97.14 kbps)
43	SCDC	HDMI-R10	+02:42:19.582164	< 23	(97.14 kbps)
44	SCDC	HDMI-R10	+02:42:19.582328	W Update_0 23	(97.14 kbps)
45	SCDC	HDMI-R10	+02:42:19.582655	R Update_0	(97.14 kbps)
46	SCDC	HDMI-R10	+02:42:19.582819	< 03	(97.14 kbps)
47	SCDCU	HDMI-R10	+02:42:19.585113	Update Reads 10:	03
48	SCDC	HDMI-R10	+02:42:19.610180	R Update_0	(97.14 kbps)
49	SCDC	HDMI-R10	+02:42:19.610344	< 13	(97.14 kbps)
50	SCDC	HDMI-R10	+02:42:19.610671	W Update_0 13	(97.14 kbps)

Type: SCDC  
Start Time: +02:42:19.610344  
Duration: 164 to 328 us  
Maximum I2C Rate: 97.14 kbps  
Read, 1 byte  
10h: Update\_0

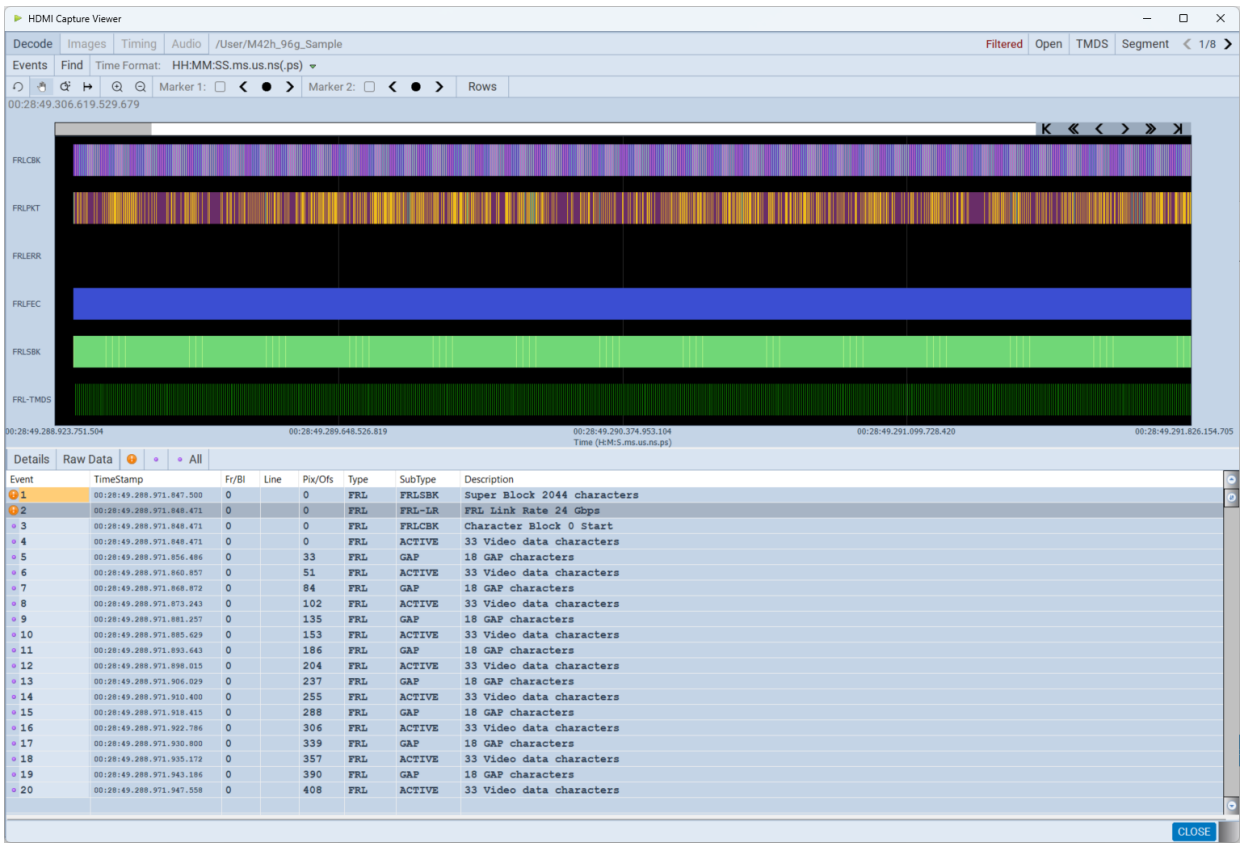
Bit	Name	Value	Description
0	Status_Update	Y(1)	
1	CBD_Update	Y(1)	
2	RR_Test	N(0)	
3	Source_Test_Update	N(0)	
4	FRL_start	Y(1)	
5	FRL_Update	N(0)	
6	...	...	
7	LIP_Update	N(0)	

\* START \*  
0000 A9 13-  
\* STOP \*

49: < 13 (97.14 kbps)

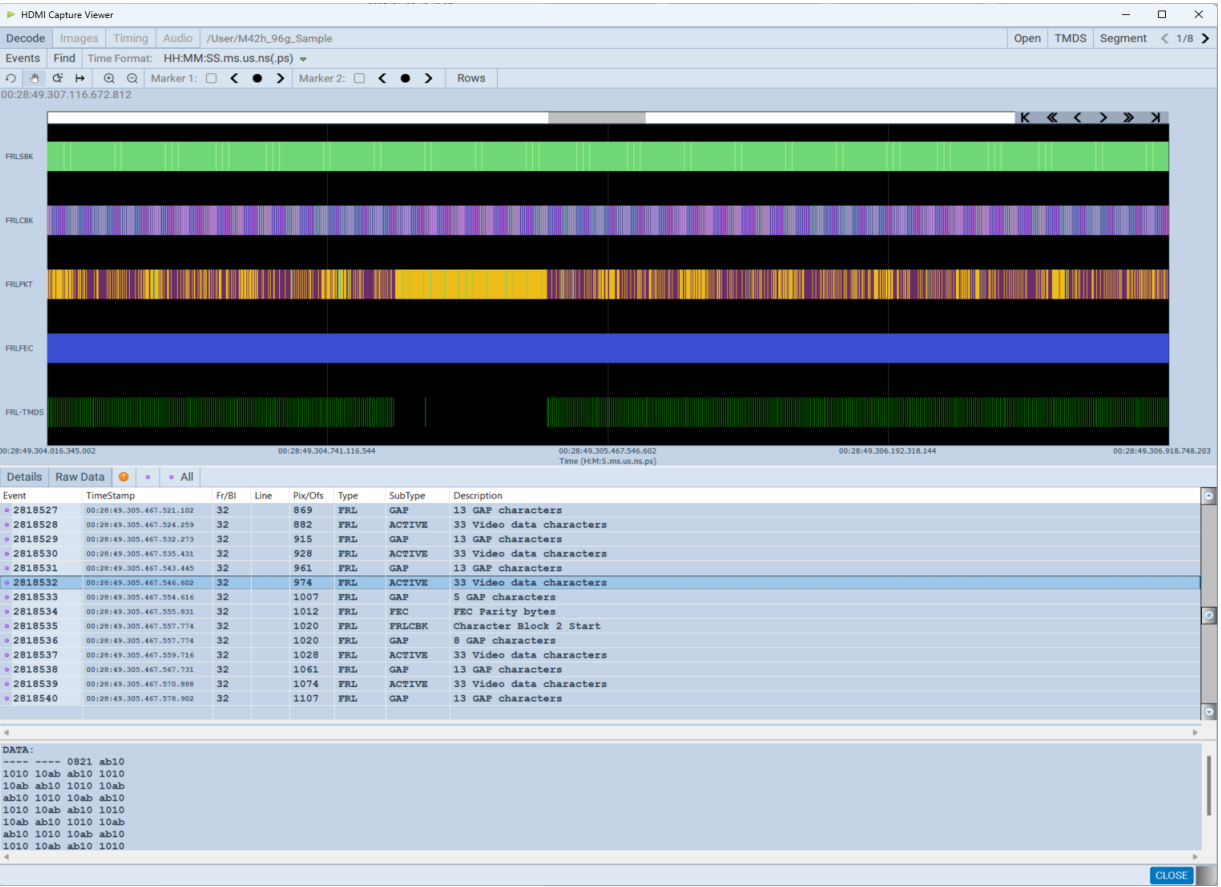
- ◆ Screen example showing FRL Link Training transactions capture at 24G per lane, 96G aggregate.
- ◆ Showing FRL Start flag set indicating source ready to transmit FRL data.

# HDMI 2.2 – M42h – Main Link Capture - FRL



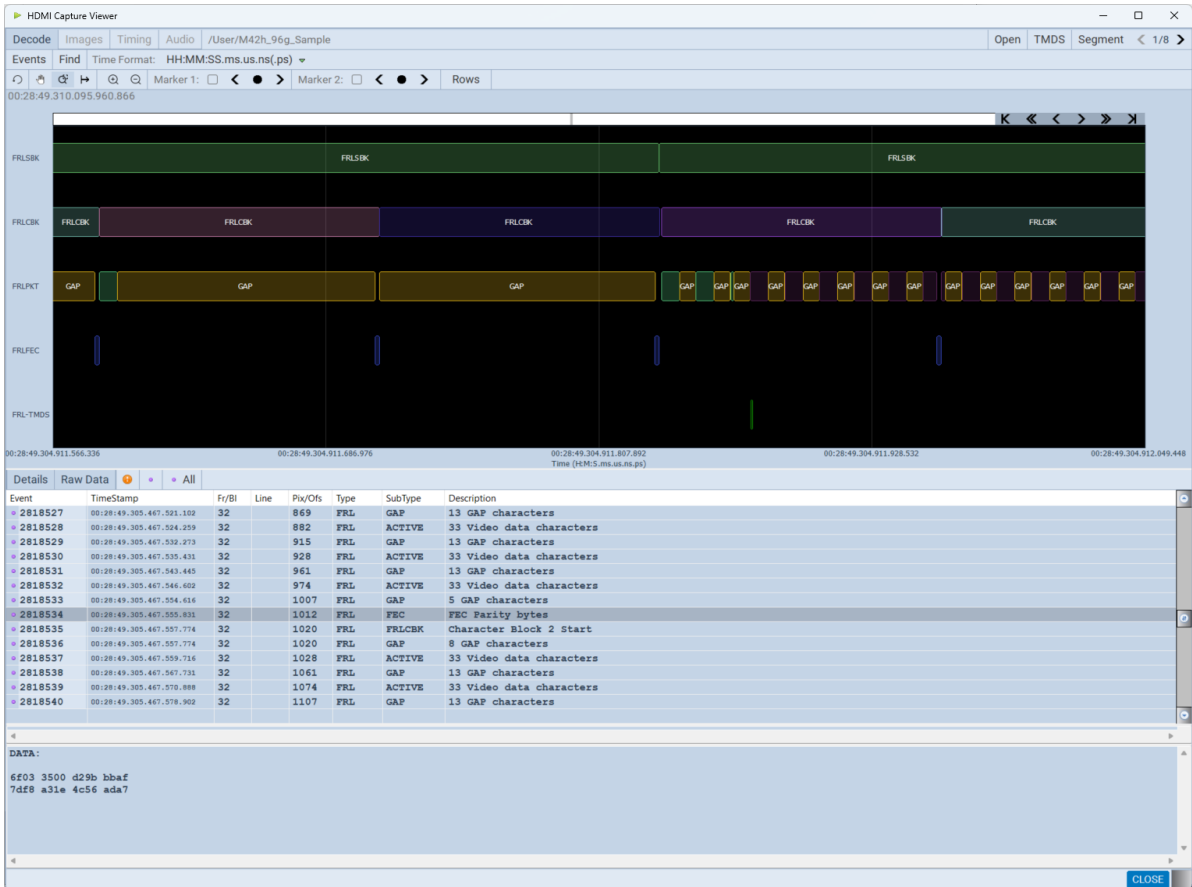
- ◆ Screen example showing FRL Main Link capture at 24G per lane, 96G aggregate.
- ◆ Showing Aggregate Link Rate of 96G.

# HDMI 2.2 – M42h – Main Link Capture - FRL



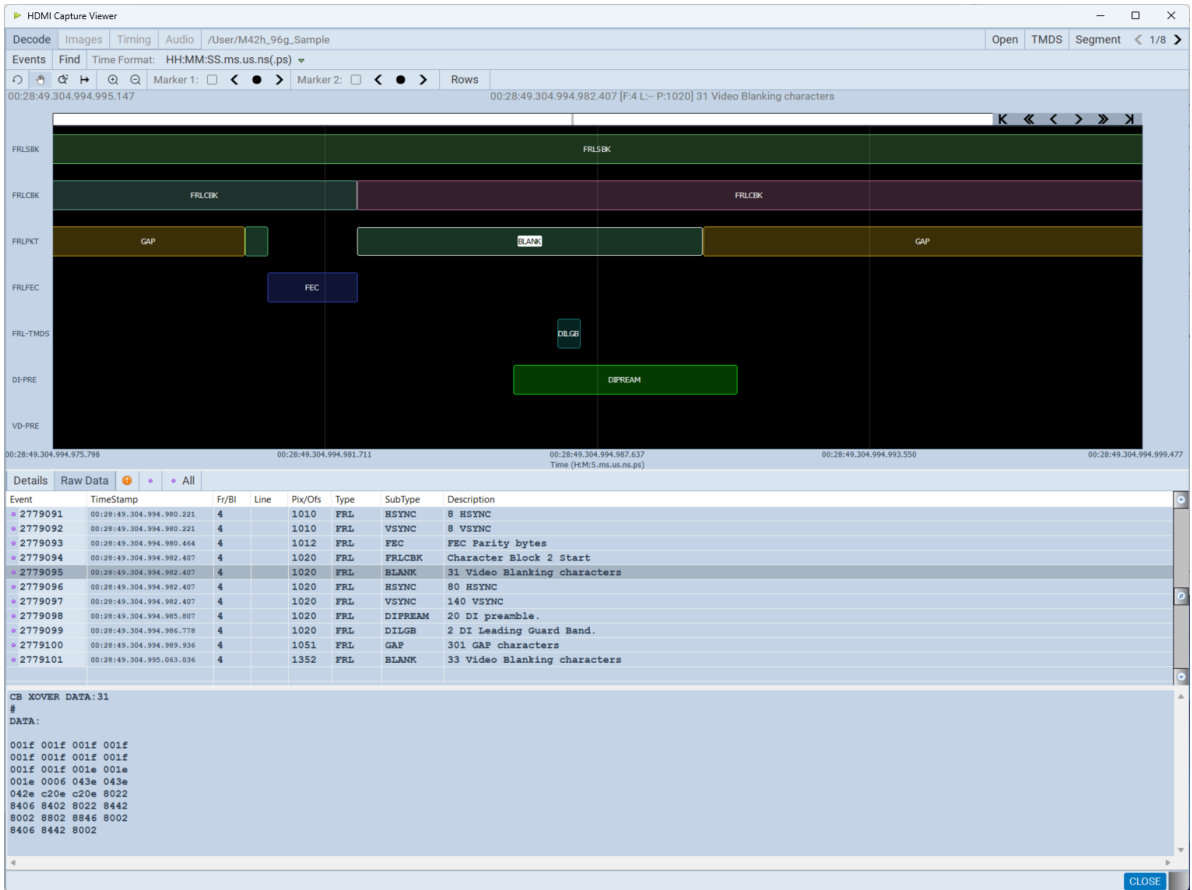
- ◆ Screen example showing FRL Main Link capture at 24G per lane, 96G aggregate.
- ◆ Showing zoomed out view of capture.

# HDMI 2.2 – M42h – Main Link Capture - FRL



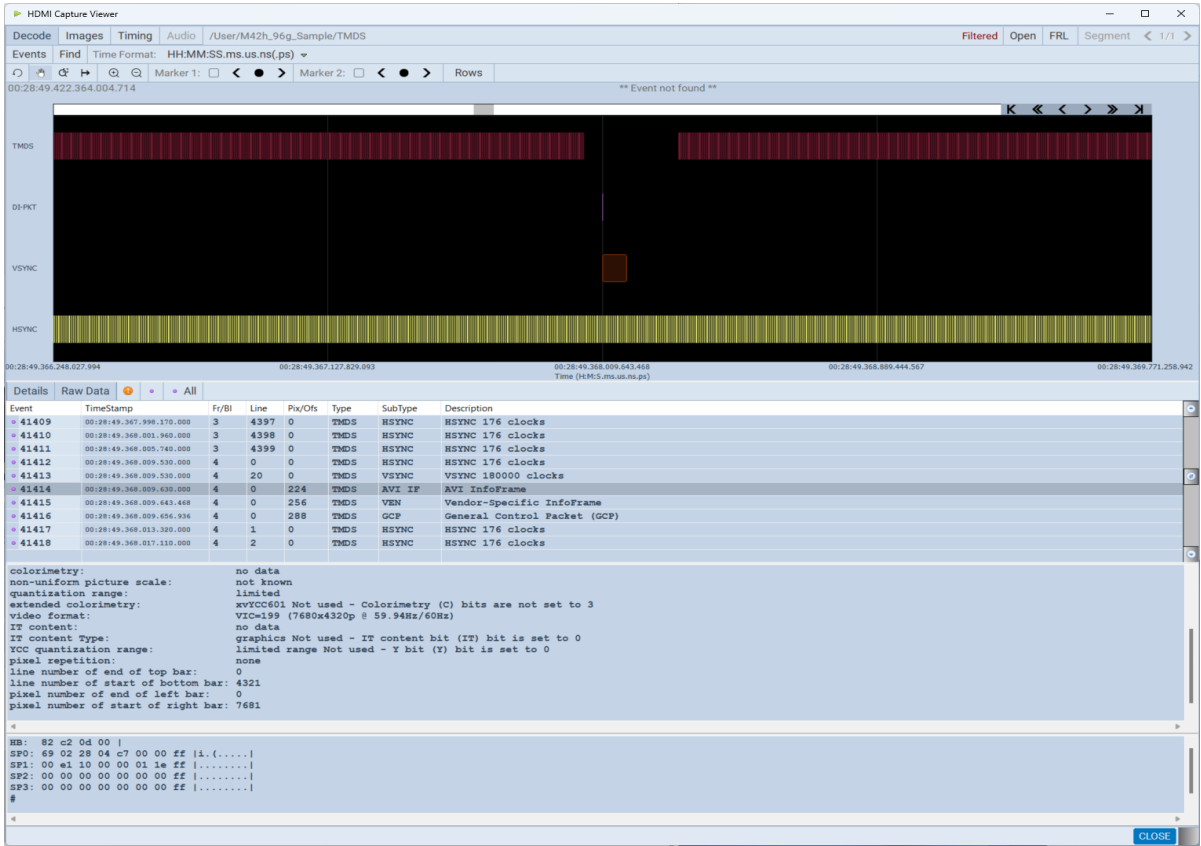
- ◆ Screen example showing FRL Main Link capture at 24G per lane, 96G aggregate.
- ◆ Showing zoomed in view of FRL structure.

# HDMI 2.2 – M42h – Main Link Capture - FRL



- ◆ Screen example showing FRL Main Link capture at 24G per lane, 96G aggregate.
- ◆ Showing zoomed in view of blanking area.

# HDMI 2.2 – M42h – Main Link Capture - TMDS



- ◆ Screen example showing TMDS view of capture.
- ◆ Showing AVI infoframe contents.

# HDMI 2.2 – M42h – Main Link Capture - TMDS

The screenshot shows the HDMI Capture Viewer interface. The top menu bar includes Decode, Images, Timing, and Audio. The main window displays a waveform with several colored blocks: AVI (purple), VEN (green), and GCP (purple). Below the waveform is a table of event details.

Event	TimeStamp	Fr/Bi	Line	Pix/Ofs	Type	SubType	Description
41409	00:28:49.367.998.170.000	3	4397	0	TMDS	HSYNC	HSYNC 176 clocks
41410	00:28:49.368.001.960.000	3	4398	0	TMDS	HSYNC	HSYNC 176 clocks
41411	00:28:49.368.005.740.000	3	4399	0	TMDS	HSYNC	HSYNC 176 clocks
41412	00:28:49.368.009.520.000	4	0	0	TMDS	HSYNC	HSYNC 176 clocks
41413	00:28:49.368.009.530.000	4	20	0	TMDS	VSYNC	VSYNC 180000 clocks
41414	00:28:49.368.009.630.000	4	0	224	TMDS	AVI IF	AVI InfoFrame
41415	00:28:49.368.009.643.468	4	0	256	TMDS	VEN	Vendor-Specific InfoFrame
41416	00:28:49.368.009.656.936	4	0	288	TMDS	GCP	General Control Packet (GCP)
41417	00:28:49.368.013.320.000	4	1	0	TMDS	HSYNC	HSYNC 176 clocks
41418	00:28:49.368.017.110.000	4	2	0	TMDS	HSYNC	HSYNC 176 clocks

check sum: invalid  
version: 194  
length: 13  
scan info: all active pixels & lines are displayed  
Bar Info: no data  
active info: no data  
RGB/YCC indicator: RGB  
active format: not defined  
picture aspect ratio: 16:9  
colorimetry: no data  
non-uniform picture scale: not known  
quantization range: limited  
extended colorimetry: xvYCC601 Not used - Colorimetry (C) bits are not set to 3  
video format: VIC=199 (7680x4320p @ 59.94Hz/60Hz)

```
##
HB: 82 c2 0d 00 |
SP0: 69 02 28 04 c7 00 00 ff |1.|.....|
SP1: 00 e1 10 00 00 01 1e ff |.....|
SP2: 00 00 00 00 00 00 00 ff |.....|
SP3: 00 00 00 00 00 00 00 ff |.....|
#
```

- ◆ Screen example showing TMDS view of capture.
- ◆ Showing zoomed in area of AVI infoframe.

# HDMI 2.2 – M42h – Main Link Capture – FRL Event Types



◆ Screen example all the FRL Event types.

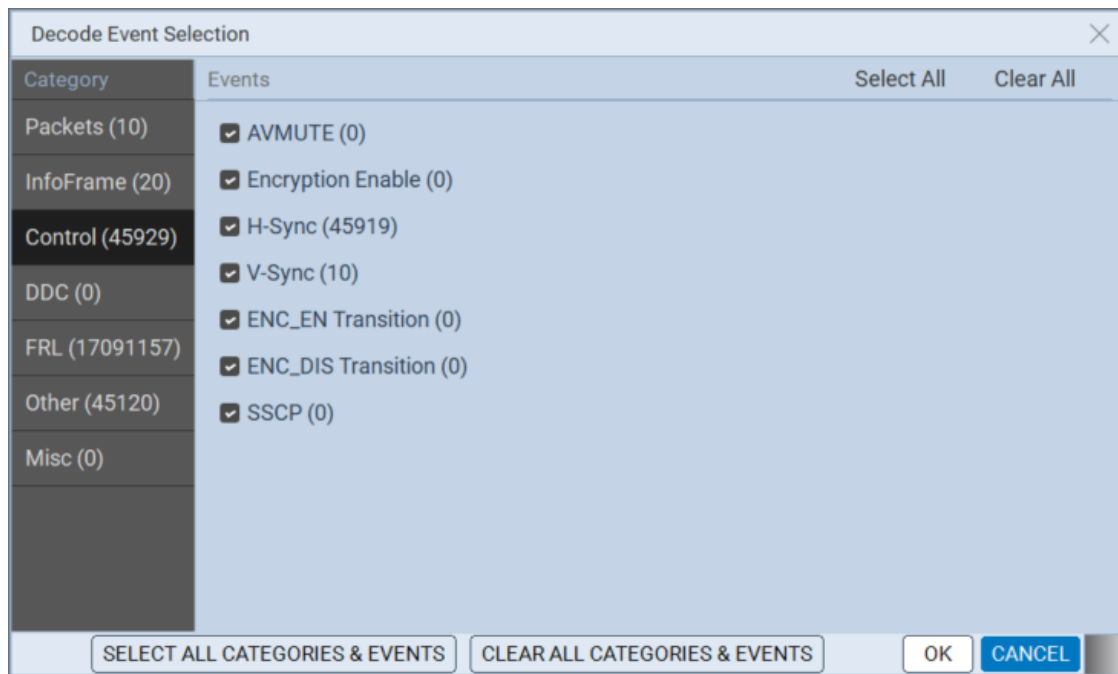
# HDMI 2.2 – M42h – Main Link Capture – TMDS Events

Category	Events	Select All	Clear All
Packets (10)	<input checked="" type="checkbox"/> Audio InfoFrame (0)		
InfoFrame (20)	<input checked="" type="checkbox"/> AVI InfoFrame (10)		
Control (45929)	<input checked="" type="checkbox"/> MPEG Source InfoFrame (0)		
DDC (0)	<input checked="" type="checkbox"/> Source Product Descriptor InfoFrame (0)		
FRL (17091157)	<input checked="" type="checkbox"/> Vendor Specific InfoFrame (10)		
Other (45120)	<input checked="" type="checkbox"/> HDR InfoFrame (0)		
Misc (0)			

SELECT ALL CATEGORIES & EVENTS   CLEAR ALL CATEGORIES & EVENTS   OK   CANCEL

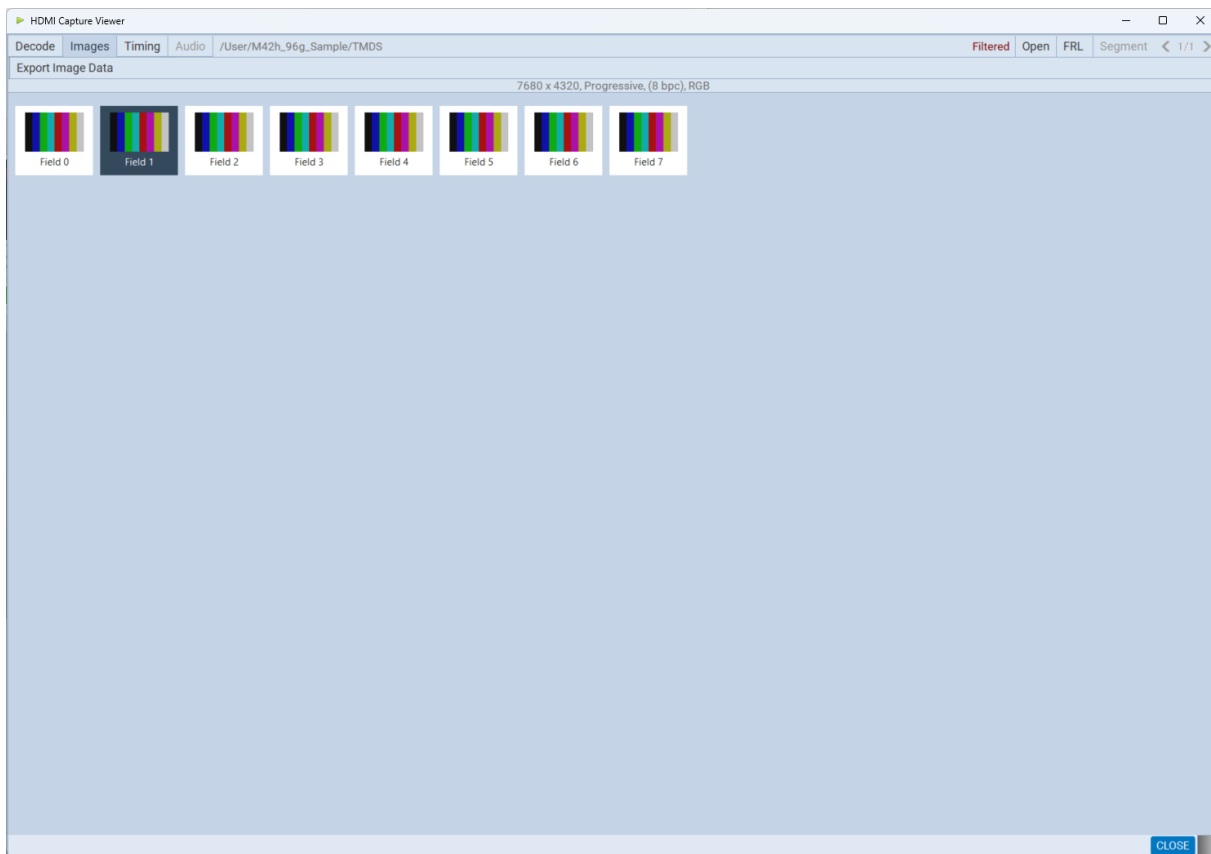
◆ Screen example all the TMDS InfoFrame Event types.

# HDMI 2.2 – M42h – Main Link Capture – TMDS Events



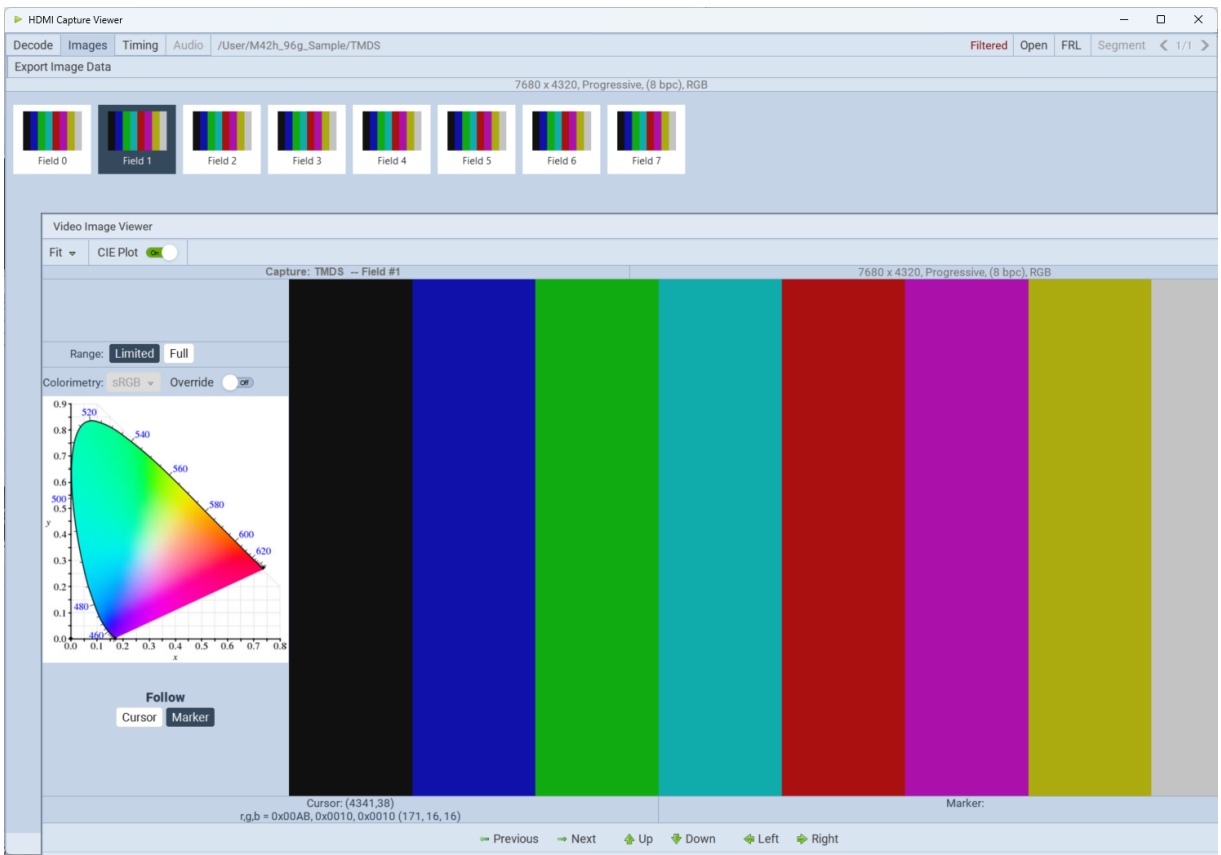
- ◆ Screen example all the TMDS Control Event types.

# HDMI 2.2 – M42h – Main Link Capture – Video Frames



- ◆ Screen example showing FRL Main Link capture.
- ◆ Viewing Video Frames captured.

# HDMI 2.2 – M42h – Main Link Capture – Video Frames



- ◆ Screen example showing FRL Main Link capture.
- ◆ Viewing a Video Frame captured.

# HDMI 2.2 – M42h – Main Link Capture – Timing Analysis

- ◆ Screen example showing FRL Main Link capture video frame and line timing.

HDMI Capture Viewer

Decode Images Timing Audio /User/M42h\_96g\_Sample/TMDS Filtered Open FRL Segment < 1/1 >

Frame Stats Line Stats

Video Format

Format	VIC	BPP	HF (kHz)	I/P	Htotal	Vtotal	Hactive	HS-F	HS-W	VActive	VS-F	VS-W	HS-P	VS-P	HToV	PF (MHz)
4320p59	199	24	264.0	P	9000	4400	7680	552	176	4320	16	1800L	Pos	Pos	0	2375.99

Frame Statistics

CTA Name	Frame	TimeStamp	Duration	VF Hz	HF kHz	Vtotal	Vactive	PF MHz	HS-W	VSync	Start Vid	HToV	Encr Start	Encr Len	Vfront	Vback
7680x4320p @ 59.94Hz/60Hz	1	00:28:49.318.009.315	00:00:00.016.666.000	60.00	264.00	4400	4320	2375.990	176	20	64	0	0	0	16	44
7680x4320p @ 59.94Hz/60Hz	2	00:28:49.334.676.054	00:00:00.016.666.000	60.00	264.00	4400	4320	2375.990	176	20	64	0	0	0	16	44
7680x4320p @ 59.94Hz/60Hz	3	00:28:49.351.342.792	00:00:00.016.666.000	60.00	264.00	4400	4320	2375.990	176	20	64	0	0	0	16	44
7680x4320p @ 59.94Hz/60Hz	4	00:28:49.368.009.531	00:00:00.016.666.000	60.00	264.00	4400	4320	2375.990	176	20	64	0	0	0	16	44
7680x4320p @ 59.94Hz/60Hz	5	00:28:49.384.676.270	00:00:00.016.666.000	60.00	264.00	4400	4320	2375.990	176	20	64	0	0	0	16	44
7680x4320p @ 59.94Hz/60Hz	6	00:28:49.401.343.009	00:00:00.016.666.000	60.00	264.00	4400	4320	2375.990	176	20	64	0	0	0	16	44
7680x4320p @ 59.94Hz/60Hz	7	00:28:49.418.009.748	00:00:00.016.666.000	60.00	264.00	4400	4320	2375.990	176	20	64	0	0	0	16	44

Line Statistics

Frame	Line	TimeStamp	Duration	HTotal	TMDS HTotal	HSync Width	HBack	HActive
3	000	00:28:49.351.346.580	00:00:00.000.003.788	9000	9000	176	0	0
3	001	00:28:49.351.350.368	00:00:00.000.003.788	9000	9000	176	0	0
3	002	00:28:49.351.354.156	00:00:00.000.003.788	9000	9000	176	0	0
3	003	00:28:49.351.357.944	00:00:00.000.003.788	9000	9000	176	0	0
3	004	00:28:49.351.361.731	00:00:00.000.003.788	9000	9000	176	0	0
3	005	00:28:49.351.365.519	00:00:00.000.003.788	9000	9000	176	0	0
3	006	00:28:49.351.369.307	00:00:00.000.003.788	9000	9000	176	0	0
3	007	00:28:49.351.373.095	00:00:00.000.003.788	9000	9000	176	0	0
3	008	00:28:49.351.376.883	00:00:00.000.003.788	9000	9000	176	0	0
3	009	00:28:49.351.380.671	00:00:00.000.003.788	9000	9000	176	0	0
3	010	00:28:49.351.384.459	00:00:00.000.003.788	9000	9000	176	0	0
3	011	00:28:49.351.388.247	00:00:00.000.003.788	9000	9000	176	0	0
3	012	00:28:49.351.392.035	00:00:00.000.003.788	9000	9000	176	0	0
3	013	00:28:49.351.395.822	00:00:00.000.003.788	9000	9000	176	0	0
3	014	00:28:49.351.399.610	00:00:00.000.003.788	9000	9000	176	0	0
3	015	00:28:49.351.403.398	00:00:00.000.003.788	9000	9000	176	0	0
3	016	00:28:49.351.407.186	00:00:00.000.003.788	9000	9000	176	0	0
3	017	00:28:49.351.410.974	00:00:00.000.003.788	9000	9000	176	0	0
3	018	00:28:49.351.414.762	00:00:00.000.003.788	9000	9000	176	0	0
3	019	00:28:49.351.418.550	00:00:00.000.003.788	9000	9000	176	0	0
3	020	00:28:49.351.422.338	00:00:00.000.003.788	9000	9000	176	0	0
3	021	00:28:49.351.426.126	00:00:00.000.003.788	9000	9000	176	0	0
3	022	00:28:49.351.429.914	00:00:00.000.003.788	9000	9000	176	0	0
3	023	00:28:49.351.433.701	00:00:00.000.003.788	9000	9000	176	0	0
3	024	00:28:49.351.437.489	00:00:00.000.003.788	9000	9000	176	0	0
3	025	00:28:49.351.441.277	00:00:00.000.003.788	9000	9000	176	0	0
3	026	00:28:49.351.445.065	00:00:00.000.003.788	9000	9000	176	0	0

Sync

CLOSE